JULY 24-27, 2023
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“Our expanding digitized world is driving unparalleled innovation across the semiconductor industry and VIPack™ represents a crucial leap forward in the transformational packaging technologies required to achieve the highly complex system integration our customers need to remain competitive,” said Yin Chang, Senior Vice President of Sales and Marketing. “Through VIPack™, we’re empowering our customers to discover new efficiencies in their semiconductor design and manufacturing process and to reimagine the integration technologies required to accomplish application excellence.”

“ASE is delighted to bring its VIPack™ platform to market, opening up new opportunities for our customers to innovate from the design process all the way to production and to reap extensive benefits in relation to functionality, performance, and cost,” said Dr. C.P. Hung, Vice President of R&D, ASE. “As the world’s leading OSAT, ASE is strategically positioned to help customers improve efficiency, speed time-to-market, and sustain profitable growth. VIPack™ underscores our commitment to deliver our most innovative packaging technologies to date.”

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CONFERENCE PROGRAM

MONDAY, JULY 24

11:00am-5:30pm  Registration Open  (Ballroom Foyer)

12:00pm-1:00pm  PDC Lunch

1:00pm-3:00pm  PDC 1: System-in-Package (SiP) - System Solutions Through Miniaturization
Mark Gerber, ASE

1:00pm-3:00pm  PDC 2: Introduction to Fan-Out Wafer Level Packaging (FOWLP)
Beth Keser, Intel Corp.  – CANCELLED

3:00pm-3:30pm  PDC Break

3:30pm-5:30pm  PDC 3: Chiplet Design and Heterogeneous Integration Packaging
John Lau, Unimicron

3:30pm-5:30pm  PDC 4: 3D Flip Chip Package Technology and Assembly Processes
Tom Dory, Fujifilm

3:30pm-5:30pm  Exhibitor Set-up  (Pine/Cedar Ballroom)

TABLETOP EXHIBITION

*Be sure to visit with our exhibitors during CHIPcon 2023!*

Tuesday, July 25 – 9:45AM-7:00PM (open during breaks, lunch, reception)
Wednesday, July 26 – 9:45AM-4:15PM (open during breaks, lunch)

**SETUP:** Monday, July 24 – 3:30PM-5:30PM; Tuesday, July 25 – 7:00AM-9:45AM
**MOVEOUT:** Wednesday, July 26 – 4:15PM-6:30PM
KEYNOTE 1: **HETEROGENEOUS INTEGRATION-RELATED GOVERNMENT FUNDING OPPORTUNITIES FOR CHIPLET ENABLEMENT IN THE AGE OF THE CHIPS ACT**

Domestic semiconductor manufacturing currently accounts for 13% of global capacity for device manufacturing at the wafer level and less than 5% at the packaging level. Facing continued deterioration of the competitive position and manufacturing posture of the domestic semiconductor industry, chiplet-enabling advanced packaging schemes centered around heterogeneous integration (HI) must find trusted domestic R&D sources as well as on-shore manufacturing outlets.

There are currently multiple US government major programs announced or contemplated for incentivizing manufacturing and nurturing future innovation in HI, but these programs are numerous and complex. This talk will provide a comparative analysis of the various funding opportunities relevant to the advanced packaging technologies required for the successful and economic execution of chiplet-based architectures. The programs to be discussed include: the National Advanced Packaging Manufacturing Program (NAPMP - part of the CHIPS Act and administered by NIST within Department of Commerce), the Electronics Resurgence Initiative (ERI 2.0) including the Next Generation Microelectronics Manufacturing program (NGMM, administered by DARPA), the Defense Procurement Act (DPA, administered by Air Force Research Lab), Strategic Transition of Microelectronics to Accelerate Modernization by Prototyping and innovate in the Packaging Ecosystem (STEAMPIPE, administered by Department of Defense), and Microelectronics Commons (parts of the CHIPS ACT and administered by Department of Defense). Program funding levels, status, timing, and intent of each will be explored through the lens of possible domestic industrial performers and beneficiaries.

**Scott Sikorski, PhD, IBM Semiconductors | ASIC, NAPMP Co-lead**

Dr. Scott Sikorski has responsibility for business development and offering management for the IBM Bromont OSAT facility as well as for driving the IBM Research Heterogeneous Integration and Chiplet ecosystem development. Previously he was responsible for developing IBM’s AI hardware partner ecosystem. He rejoined IBM in 2020 after a decade in the broader industry. He is based out the T.J. Watson Research Center.

Prior to his return to IBM, Dr. Sikorski was with STATS ChipPAC for 10 years. During this time he held leadership positions in product line management and business development before being promoted to head of Corporate Strategy in late 2012. In this role he assisted in the acquisition of the company by JCET Group in 2015. In JCET, he was named Vice President of Product Technology Marketing and in December 2017, Dr. Sikorski was appointed VP of Group Technology Strategy.

Dr. Sikorski served on the Boards of Directors of industry organizations INEMI and MEPTEC for several years. The International Electronics Manufacturing Initiative (iNEMI) is a not-for-profit, R&D consortium forum focused on accelerating improvements in the electronics manufacturing industry. MEPTEC, the MicroElectronics Packaging and Test Engineering Council, is a trade association of semiconductor suppliers, manufacturers and vendors engaged in packaging, assembly and test.

Dr. Sikorski started his career in 1989 with IBM Microelectronics holding positions in R&D, manufacturing, product line management, business development and complex deal negotiation over a 20-year period. He received his Bachelor of Science degree from Columbia University’s School of Engineering and Applied Sciences in Metallurgical Engineering and his Master’s degree and Ph.D. from the Massachusetts Institute of Technology, both in Materials Engineering.

KEYNOTE 2: **NEW LEVEL INNOVATION OF ADVANCED HETEROGENEOUS INTEGRATION**

Breakthroughs in AI, 5G, autonomous vehicles and Metaverse tech promise to reshape the way we live -- but delivering the function and performance to power those advancements on a single chip is becoming more complex, and less cost-effective. Advances in heterogeneous chip packages are needed to empower today’s device manufacturers to pursue tomorrow’s breakthroughs. Both 2.xD and 3D variations will be needed to keep the innovation vibrant. 3DIC packages save massive amounts of on-chip real estate by stacking components vertically, reducing surface area and bumping performance by shortening the space between chips.

This presentation shares Samsung AVP Platform including X-Cube, I-Cube and FOPKG as full multi-die integration solutions, in terms of technology roadmap, challenges and opportunities for emerging high-end computing, memory and mobile applications. Besides, here we would like to discuss about the latest activities of advanced PKG and UCIe chiplet standardization, and industrial collaboration in ecosystem across all chip companies, design partners and foundries in the ecosystem for effective system integration and product innovation.

**Vincent (WooPoung) Kim, Samsung Electronics | Corporate EVP / Head of Advanced Packaging in SAMSUNG-DSRA**

Dr. KIM is currently working as Corporate EVP / Head of DSRA-AVP in San Jose, CA. SAMSUNG has launched a new business unit to support the need of the semiconductor industry’s advanced packaging for higher-performance systems. The name of the new business is AVP (Advanced Packaging). Prior to joining Samsung, he was system architect for Signal Integrity and Power Integrity at Apple, path-finding to build leading-edge consumer computers. Previously, he was with Qualcomm as SI manager in Snapdragon packaging. Earlier than Qualcomm, he worked as co-design engineer at Wireless Business Unit of Texas Instruments working to optimize the electrical design of OMAP packages/systems. Before TI, he was with Rambus as SI engineer to design and analyze memory systems. Dr. Kim received Ph.D Degree in ECE at Georgia Tech in 2004 and M.S. & B.A. degrees from KAIST, Korea in 1999 and 1997.
9:45am-10:30am  
(Pine/Cedar Ballroom)

**Coffee Break & Networking in Exhibits sponsored by**

9:45am-7:00pm  
(Pine/Cedar Ballroom)

**Exhibits Open**

9:45am-10:30am  
(Pine/Cedar Ballroom)

**Session 1:**  
**CHIPLET INTEGRATION WORKFLOWS AND CO-DESIGN**

**Session Chair:** John Park, Cadence

10:30am-11:00am

**Petaflops AI Neural Processor on Chiplet Heterogeneous Integration Package**
Youngsu Kwon, ETRI

11:00am-11:30am

**Workflows for tackling heterogeneous integration of chiplets for 2.5/3D**
Kevin Rinebold, Siemens

11:30am-12:00pm

**Hierarchical Device Planning methodology and workflow for heterogeneously integrated chiplets and ASICs**
Zain Ali, Intel

12:00pm-1:30pm  
(Pine/Cedar Ballroom)

**Lunch & Networking in Exhibits sponsored by**

**Session 1 continued:**  
**CHIPLET INTEGRATION WORKFLOWS AND CO-DESIGN**

**Session Chair:** Kevin Rinebold, Siemens

1:30pm-2:00pm

**Chiplet/Package Co-Design/Analysis Challenges and Opportunities**
John Park, Cadence

2:00pm-2:30pm

**Integrated power integrity analysis workflows for heterogeneous package design**
Jeff Cain, Chipletz

2:30pm-3:30pm  
(Pine/Cedar Ballroom)

**Coffee Break & Networking in Exhibits sponsored by**

3:30pm-4:00pm

**A Novel Strategy to Mixed Memory System-in-Package Co-Design**
Matt Monroe, Micron

4:00pm-4:30pm

**Using package assembly planning to enable system-level codesign, netlisting and assembly LVS**
Magesh Govindarajan, Qualcomm

4:30pm-4:45pm

**Short Break**
We put **Advanced Packaging** to the test.

Amkor’s advanced System in Package (SIP) solutions enable highly integrated products in a smaller footprint with higher component density and increased system performance. Innovative test solutions help deliver quality and reliability for all your advanced SIP packaging needs.

Enabling the Future

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Panel Session: ARE CHIPLETS THE ANSWER FOR AI, ML AND PHOTONICS/CPO? 
Moderator Jan Vardaman, TechSearch International
Confirmed Panelists:
Ivor Barber, AMD
Yin Chang, ASE, Inc.
Swadesh Choudhary, Intel Corp.
Mike Kelly, Amkor Technology
Chong Zhang, Ayar Labs

Conference Reception with the Exhibitors sponsored by

WEDNESDAY, JULY 26

Session 2:  
FINE PITCH BONDING TOOLS AND PROCESSES 
Session Chair: Eelco Bergman, Saras Micro Devices

8:00am-8:45am  KEYNOTE 3:  
DIE TO WAFER HYBRID BONDING FOR HETEROGENEOUS INTEGRATION
Chip to wafer Hybrid Bonding plays a key enabling role for advanced Heterogeneously Integrated products. This new assembly technology runs in high volume with key providers and significant growth is projected. Examples of the production use of the technology will be provided as well as the equipment capability required to enable sub-5 micron I/O pitch. A successful Hybrid bonding process requires a diverse set of equipment and well controlled processes beyond just the capability of an accurate die bonder. The presentation will cover the driving factors supporting the growth of chip to wafer Hybrid bonding, examples of production applications, and the key processes used to enable the assembly technology. 

Tom Strothmann, Besi North America, Inc. | VP of Sales and Service North America

8:45am-9:15am  Fluxless Thermocompression Bonding via in-situ Oxide Reduction
Peter Van Emmerik, Kulicke & Soffa Industries

9:15am-9:45am  Assembly Solutions for Cost-Effective Heterogeneous Integration with Disparate Die Types
Glenn Farris, Universal Instruments
9:45am-10:30am  Coffee Break & Networking in Exhibits sponsored by:
(Pine/Cedar Ballroom)

9:45am-4:15pm  Exhibits Open

Session 3:  Fir/Oak Ballroom
CHIPLET PACKAGE ASSEMBLY, MATERIALS, AND PROCESS TECHNOLOGY
Session Chair: Christo Bojkov, University of Texas, Dallas

10:30am-11:00am  IBM Advanced Packaging solutions in North America
Alexander Janta-Polczynski, IBM Bromont

11:00am-11:30am  Advanced Insulation Materials Designed for High-Density Package for High Speed Application
Ryohei Ooishi, Ajinomoto

11:30am-12:00pm  Co-Designed and Co-Integrated 3D Electronic and Photonic Integrated Circuits realized by DBI® for Energy-Efficient and High-Throughput Optical Interconnects
S.J. Ben Yoo, University of California, Davis (Anirban Samanta, Mingye Fu, Mehmet Berkay-On, Yu Zhang, University of California, Davis; Po-Hsuan Chang, Peng Yan, Ankur Kumar, Hyunryul Kang, Il-Min Yi, Dedeepya Annabattuni, Yang-Hang Fan, Yuanming Zhu, Samuel Palermo, Texas A&M University; David Scott, Optelligent; Robert Patti, Nhanced Semiconductors)

12:00pm-12:30pm  Carbon-Based Thermal Interface Materials for High-Power Device Packaging
Kevin Brenner, University of Texas, Dallas

12:30pm-1:45pm  Lunch & Networking in Exhibits sponsored by
(Pine/Cedar Ballroom)

Session 4:  Fir/Oak Ballroom
ADVANCED SiP PACKAGING FOR MOBILE AND WEARABLE
Session Chair: Mark Gerber, ASE US

1:45pm-2:30pm  KEYNOTE 4  (Fir/Oak Ballroom)
EXTENDING MOORE’S LAW WITH CHIPLET INNOVATION
Moore’s law has been the backbone of the digital evolution, but as silicon process technology complexity scales up, silicon process technology is now approaching the physical limitation and Moore’s law is slowing down for almost all products that rely on transistor scaling for its future evolution. Also, with increasing process complexity, the silicon wafer price is expected to continue increasing. Slowing transistor scaling together with increasing wafer price lead to increasing transistor cost, which is a big problem for future feature growth roadmap for multiple semiconductor products. To continue supporting feature growth in cloud computing, edge computing, IoT, mobile, and XR, it is inevitable to adopt chiplet approach down the road. The AI evolution now requires even higher feature growth rates not only for cloud computing devices but also for edge devices. The chiplet approach has been mainly adopted in HPC, but with slowing Moore’s law, we foresee the strong need for chiplet adoption in more edge and mobile devices too. Cost-effective and package form factor-friendly chiplet integration solutions are key for expedited chiplet adoption to mobile devices. The presentation will cover key considerations and options for mobile chiplet integration solutions and key challenges and hurdles to overcome.

Jihong Choi, Qualcomm Technologies, Inc., | Principal Engineer
Since joining Qualcomm process technology and foundry engineering team in Jan 2012, Jihong has worked on pathfinding, customization, NPI, and early process settlement for new foundry technology nodes for the last 11 years. Working in the front line to extend Moore's law for Qualcomm’s silicon process solutions, he is currently leading the heterogeneous integration and passive device development team in process technology and foundry engineering org. Before joining Qualcomm, he worked as a process development engineer at AMD's advanced process technology team and as a DFM/OPC engineer at GlobalFoundries. He has over 17 years of semiconductor technology development experience and holds Ph.D. in Mechanical Engineering from UC Berkeley.

2:30pm-3:00pm  Heterogeneous Integration Design Flow for Radio Front Ends
Matthew Poulton, Qorvo

3:00pm-3:30pm  Next Generation 5G mmW Module Architecture
Tilson Chung, ASE, Inc.
Our world runs on semiconductors — from the smartphones in our hands to the powerful systems that underpin generative AI. Today, no aspect of the economy is untouched by semiconductors, and for decades, chips have grown smaller and faster, exponentially increasing the amount of processing power available to us. These technologies make our societies faster, smarter, more productive, and more innovative.

But now, the semiconductor industry has grown heavily centralized. As we enter the age of AI and the demand for compute surges, our supply chains are fragile, and the environmental impact is growing. Meanwhile, Moore's Law is approaching its limit. For progress to continue, we need new approaches, new architectures, new materials — and new collaborations.

Join us in building a semiconductor industry for all of tomorrow’s challenges.
Session 5: Fir/Oak Ballroom
AUTOMOTIVE, POWER & SENSOR PACKAGING
Session Chair: Curtis Zwenger, Amkor Technology

4:15pm-4:45pm  Power Packaging and Integration for Automotive Applications
KyungSu Kim, Amkor Technology

4:45pm-5:15pm  Power Module Packaging Trends for EV Traction Inverters
Roveendra Paul, onsemi

5:15pm-5:45pm  New generation of gas sensors: anticipated and unanticipated advantages over last-century sensor designs
Radislav Potyrailo, GE Research

6:30pm-8:30pm  Offsite Networking Reception & Beer Tasting at
FAULTLINE MICROBREWERY | 1235 Oakmead Pkwy., Sunnyvale, CA 94085
Bus departs from the CHIPcon hotel at 6pm. Will return leaving Faultline at 8:30pm
Includes transportation, unlimited beer tasting (5 varieties), food, tax/gratuity
Tickets are $75 per person – Space Very Limited
Register at IMAPS Registration Desk Right Away
THURSDAY, JULY 27

7:00am-12:00pm
Registration Open
(Ballroom Foyer)

Conference Breakfast Sponsored by:

IBM

8:00am-8:15am Final Day Opening comments – General Chairs

Session 6: Fir/Oak Ballroom
TEST, METROLOGY AND DATA ANALYTICS
Session Chair: Jeorge Hurtarte, Teradyne

8:15am-8:45am Path towards zero defects: re-evaluating HVM metrology sampling strategies
Frank Chen, Bruker

8:45am-9:15am Developing a process to design multi-site, high-volume OTA test solutions for Antenna-In-Package (AiP) RF devices
Eric Shoemaker, Teradyne

9:15am-9:45am Testing at the Edge - How Chiplets and Heterogenous Integration are Driving the Need for Real-Time Decisions During Test
Ira Leventhal, Advantest America, Inc.

9:45am-10:30am Coffee Break
(Ballroom Foyer)

Session 7: Fir/Oak Ballroom
CHIPLET INTEGRATION INTERFACE STANDARDS
Session Chair: Steven Kummerl, Texas Instruments

10:30am-11:00am The New Open Chiplet Economy
Bapi Vinnakota, Open Compute Project (OCP)

11:00am-11:30am UCIe™: An Interconnect Standard to Enable an Open Chiplet Ecosystem
Gerald Pasdast, UCIe Consortium Form Factor and Compliance Workgroup Co-Chair and Senior Principal Engineer at Intel

11:30am-12:00pm A Design Approach Promoting Sustainability, Shorter Time to Train/Infer and Lowers TCO
Patrick Soheili, Eliyan

12:00pm Closing Remarks

Thank you to our CHIPcon 2023 Exhibitors!

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