ADVANCED SYSTEM IN PACKAGE TECHNOLOGY
VIRTUAL CONFERENCE

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August 9-12, 2021
A GLOBAL VIRTUAL CONFERENCE!

The top global virtual event for Advanced System-in-Package technologies!

Combining the 3D ASIP and IMAPS SiP events into an exciting, comprehensive program:
One event covering SiP technology developments, solutions and business trends.

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Nozad Karim, Amkor Technology
Jan Vardaman, Tech Search Intl.
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Optional Professional Development Courses for further education (additional reg required)

Available On-Demand starting August 6 for 30 days.

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Heterogeneous Integration Roadmap (HIR) Workshop

10am-2:30pm Eastern

HIR Workshop

Organizing Committee: Chair – William Chen, Co-Chairs – WR Bottoms, Vikas Gupta

The Heterogeneous Integration Roadmap (HIR) is a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration between industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of Emerging Research Devices and Emerging Research Materials with longer research-and-development timelines. The HIR is sponsored by three IEEE Societies (Electronics Packaging Society, Electron Devices Society & Photonics Society) together with SEMI and ASME Eeelctronics & Photonics Packaging Division.

This HIR workshop @ IMAPS SIP Conference will start with a guest keynote to highlight future challenges from automotive electronics industry perspective. We shall then feature seven selected topics from the HIR chapters including an overview presentation. The purposes for the HIR workshop at IMAPS SIP Conference are to feature technology innovation & advancements & stimulate collaboration around the world.

- Welcome - IMAPS SIP Conference Host
- Keynote Speaker Introduction - William Chen
- Keynote : Automotive Packaging – System Integration and Reliability - Thorsten Meyer (Infineon)
- Introduction to HIR Workshop - IMAPS SIP Conference HOST
- HIR Overview - William Chen & WR Bottoms (3MTS)
- Automotive Electronics - Rich Rice (ASE), Veer Dhandapani (NXP)
- Break
- SiP & Module - R. Aschenbrenner (IZM), Klaus Pressel (Infineon), Erik Jung (IZM)
- MEMS & Sensor Integration - Shafi Saiyed (Analog Devices)
- Integrated Power Electronics - Cian O’Mathuna (Tyndall)
- Modelling & Simulation - Christopher Bailey (Greenwich U) & Xuejun Fan (Lamar U)
- Reliability - Abijit Desgupta (U Md), Richard Rao (Inphi), Shubhana Sahasrabudhe (Intel)
- Workshop Q&A and Workshop Completion William Chen, Bill Bottoms & Vikas Gupta

2:30-4:30pm Eastern

PDC: System-in-Package (SiP) - System Solutions Through Miniaturization

Mark Gerber, ASE US

This PDC course will introduce the package platform SiP (System-in-Package) and how some companies are diversifying from SOC (System-on-a-Chip) to leverage heterogeneous silicon integration and package miniaturization to enable system level solutions. A short market perspective will be reviewed as well as how industry segments are leveraging SiP and how the OEM market is evolving and creating system level ecosystems to enabling content revenue- a key area of IOT. SiP general process flow details will be covered as well as key process considerations for yield improvements. In addition, a brief overview of some of the tools that may be leveraged to help miniaturize module solutions and improve performance. This class will also introduce several variations of the SIP platform using Fan-Out Wafer Level packaging and new embedded substrate technologies are also emerging as powerful future platforms to enable lower power and higher performance devices using solderless interconnects.
ISO & TS-16949 Certified
AECQ-Certified Packaging
ZERO PPM Quality Policies
Power-Discrete Packaging
HVM-Proven ADAS Solutions
SiP Solutions for 5G/IoT — SiP Solutions for Automotive, Industrial & Power

10:00am-10:15am Eastern
Introduction to Day 2 Keynotes

10:15am-11:00am Eastern
KEYNOTE: 5G Paves the New Phase of the Packaging Technology
Choon Lee, JCET Group

5G is going to allow most high bandwidth users to access their mobile radio communication more efficiently. It can be possible through new or enhanced packaging technologies that include denser form factor-oriented and antenna embedded/separated structures. This talk will share the 5G related packaging technologies which enable 5G mobile products to be accommodated within allowed board space.

11:00am-11:45am Eastern
KEYNOTE: On the Development of mmW Surface Mount Antenna for Automotive SIP Wireless Products at the Network Edge
Joy Laskar, MAJA Systems

There has been growing interest in adoption of millimeter-wave technology for high-speed data transport to compliment current enterprise technologies, such as optical and metal-based interconnects, offering substantial advantages in bandwidth, reach, power consumption, and cost. It has been only recently, with the emergence of mmW radio ICs in combination with innovative antenna technology that one can envision a new class of systems and applications for low delay and high...
throughput connectivity. In this presentation, we focus on recent breakthroughs in Surface Mount Antenna technology enabling wireless SIP products for automotive customers at the edge of the network providing solutions for wireless data ingestion, improved connectivity and signal integrity.

12:00pm-1:00pm Eastern
**Panel Session: SiP Challenges for 5G**
The 5G rollout is underway for both sub 6GHz and mmWave. The design, fabrication, and test of SiPs, especially to support mmWave 5G applications, present challenges. This panel will discuss issues including design, materials, and test.

*Panelists: Michael Liu, Director, JCET Group; Nozad Karim, Amkor Technology; Mark Gerber, ASE; Tanja Braun, Fraunhofer; David Vye, Cadence*

*Moderator: Jan Vardaman, TechSearch International*

2-4pm Eastern
**PDC: 5G mmWave package development requirements and solutions**
*Urmi Ray, Consultant*
The seventh Generation (5G) mobile communication era is expected to address the insatiable need for data communication by introducing mmWave technology and protocols. The unprecedented latencies offered by 5G Networks will enable users to indulge in gigabit speed immersive services regardless of geographical and time dependent factors.

The key to enabling this architecture is packaging and system integration, especially involving an effective antenna structure and RFIC communication in cost-effective, small form-factor packages. As full speed development, demonstration and qualification of mmWave systems have accelerated in 2017, different design and packaging architectures are emerging.

This PDC will provide a comprehensive landscape of package development options including LTCC, eWLB/FOWLP as well as laminate based packaging. The specific requirements of materials and process needs (low dielectric material, copper roughness requirements) are discussed. Multiple different package structures are presented as case studies to demonstrate comparative performance of eWLB vs laminate packages. Product application spaces ranging from mobile/handheld to network infrastructures and automotive/satellite radars are highlighted. Key aspects and guidelines towards a cost/performance trade-off analysis will be summarized.

4-6pm Eastern
**PDC: Substrate for Heterogeneous Integrations (SiPs)**
*John Lau, Unimicron Technology Corporation*
Heterogeneous integration or SIP (system-in-package) uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (side-by-side and/or stack) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem. For the next few years, we will see more implementations of a higher level of heterogeneous integration, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in chiplets and heterogeneous integrations will be presented. The lecture materials are mainly from the papers from others and the latest books (Heterogeneous Integrations 2019 and Semiconductor Advanced Packaging 2021) authored by the lecturer and every attendee will receive more than 120 pages of lecture handouts.
WEDNESDAY, AUGUST 11

Wearables/Medical — SiP EDA/Design/Modeling

10:00am-10:15am Eastern
Introduction to Day 3 Keynotes

10:15am-11:00am Eastern
KEYNOTE: Ever Smaller: The Increasing Viability of SiPs in Consumer Electronics
Pieris Berreitter, Fitbit/Google

The wrist of the average human has changed very little over the course of human history; meanwhile, our expectation of what’s possible in a watch seems to have no bounds. As this appetite for features increases we are compelled as product developers to focus our miniaturization lens beyond the obvious targets. This talk will cover some classical SiP solutions as well as some less obvious candidates, addressing challenges unique to the consumer electronics industry. While the examples we will cover in this talk are derived from smartwatches, the fundamental elements apply to all space-constrained designs.
Advanced SiP Packaging at Amkor

Amkor’s advanced System in Package solutions enable highly integrated products with performance advantages, smaller footprint, higher component density and increased overall system performance.

Enabling the Future

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11:00am-11:45am Eastern
KEYNOTE: Chiplets and Heterogeneous Integration Bring a New Twist to SiP
Keith Felton, Siemens EDA

The semiconductor industry is facing an inflection point as higher cost, lower yield, and reticle size limitations drive the need for viable alternatives to traditional monolithic solutions, which have hit the limits of physics. This is driving an emerging trend to disaggregate what typically would be implemented as an SoC into solid, fabricated IP blocks, otherwise known as chiplets. These chiplets typically include just a couple of functions implemented at the optimal process node, when combined with other chiplets, memory and often a custom ASIC results in a multi-die heterogeneous integrated implementation that typically utilizes a high-performance substrate ushering in a new generation of system-in-package and with it a new set of design challenges that we will explore.

12:00pm-1:00pm Eastern
Panel: Solving Complex Design Challenges in HI and SiP
Moderator: Urmi Ray, Consultant
Panelists: Javi DeLaCruz, ARM and George Harris, Amkor Technology

ON-DEMAND — See full description after agenda

Wearables/Medical
SiP market and technology trends for wearables applications
Santosh Kumar, Yole
Bio-sensing and its Integration in Wearables
Henry Lin, ASE Group
Applying Silicon Photonics to Health Sensor Technology
Dave McCann, Rockley Photonics

SiP EDA/Design/Modeling
Strategies for 2.xD and 3D Integration
Javi DeLaCruz, ARM
Design Flow Challenges for Silicon-centric Multi-chip(let) Packages
John Park, Cadence
Ansys: Solving the Unsolvable
Kevin Quillen, ANSYS
THURSDAY, AUGUST 12

HPC/SiPh, Chiplet Integration — SiP Test & Yield Enablement

10:00am-10:15am Eastern
Introduction to Day 4 Keynotes
2022 SiP Conference, IMAPS International, Other IMAPS Announcements, Wrapup

10:15am-11:00am Eastern
KEYNOTE: From 5G mmWave to 6G THz: What’s Next in RF Test Challenges?
Jeorge Hurtarte, Teradyne

As each G in mobile networks generations takes about eight years to follow the previous one, we’re only about five years from facing new 6G THz test challenges. And given that 5G mobile networks are just ramping up with high volume millimeter wave devices, is it too early to start worrying about 6G test challenges? This presentation starts with an overview of the possible 6G use cases that make THz a requirement as we enter into the second half of this decade and then follows with a preview of the test challenges that can be expected for 6G beyond the current 5G millimeter wave test challenges.

11:00am-11:45am Eastern
KEYNOTE: Optical I/O Chiplets for Next-Generation Heterogeneous Computing
Mark Wade, Ayar Labs

Electrical communications technologies are facing challenges in scaling bandwidth while achieving compelling energy efficiency, bandwidth density, latency, and reach. While digital processing performance continues to scale in how much compute can be achieved per unit area of silicon, the ability to fuel processing cores with bandwidth has become a major limiting factor for many high-value workloads, such as machine learning. A new I/O technology is needed that can match the performance requirements needed for computing fabrics and have a viable path to scale to high-volumes. In this talk, we present progress towards a new generation of densely integrated optical I/O technologies that address the bandwidth density, energy efficiency, and scalability requirements for next-generation computing fabrics and demonstrate a new overall chip-to-chip I/O architecture based on this technology.

12:00pm-1:00pm Eastern
Panel Session on HPD/Chiplet Integration
Moderator: Eelco Bergman, ASE Group
Panelists: Jeorge Hurtarte, Teradyne and Ravi Agarwal, Facebook

2-4pm Eastern
PDC: 3D Packaging Assembly and Technology for Mobile Devices
Tom Dory, Fujifilm

This PDC provides details on current and future assembly 3D packaging processes and technologies. The 3D IC and wafer-level packaging area is forecasted to grow to over $170 billion by 2022 driven by mobile devices including phone, tablet and laptop computers and gaming devices. Advanced packaging requirements require the evolution of back end manufacturing to become more process control driven. The 3D stacked die TSV packaging has advantages, but only in some market segments.
In the cell phone market, stacking chips helps to minimize some of the interconnect issues between the logic and the memory chips. Wire bonding remains a key assembly method for 3D memory packages with a separate assembly process flow.

This PDC will cover 3D and 2.5D (interposer) designs, 3D assembly flow, known good die, KGD, concerns, 3D package testing issues, supply line logistics, thermal management, logic bump out designs, wafer thinning and handling (thermal & laser debonding and residue removal) and interposers with microfluidics cooling built-in. The objective of this PDC is to provide the students with an overview of the technologies, materials, and processes involved in the latest 3D and 2.5D assembly processes.

**ON-DEMAND — See full description after agenda**

**HPC/SiPh, Chiplet Integration**

**Packaging Challenges and Opportunities for mmWave Communications**
Dr. Madhavan Swaminathan, Georgia Tech

**Facebook Data Centers Heterogenous Integration Driven by AI/ML and Network Applications**
Ravi Agarwal, Facebook

**Advanced Die Attach Technologies for the Chiplet Era**
Chris Scanlan, Besi

**SiP Test & Yield Enablement**

**SiP Test Solution for 5G/IoT**
Vineet Pancholi, Amkor Technology

Minimizing deleterious radiation effects in sensitive CMOS devices while maintaining 100% coverage strategies for X-ray defect inspection in double-sided SiP manufacturing
Francisco Machuca, SVXR

**Overview of Warpage and Void Simulations for System in Package (SiP)**
Eric Ouyang, JCET

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**Soldering Materials for Heterogeneous Integration and Assembly**

- 3D Logic / Memory and Flip-Chip
- System-in-Package
- Thermal Interface Materials
- Ball Grid Array
- SMT

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SiP Solutions for 5G/IoT
Implementation of 5G mmWave from Module to System Integration
Li-Cheng Shen, Universal Global Scientific

Miniaturization of 5G mmWave modules has brought it to compact handheld devices. In addition to mechanical matching, how to manage performance, latency, reliability, and efficiency in system integration has become the key to success in end-product development. In this talk, a practical implementation from mmWave module characterization to system integration and verification on a ruggedized 5G handheld device development will be presented.

Novel Materials for Fine RDL and 5G Applications
Habib Hichri, Ajinomoto

Build-up process is a highly effective for high-density integration of printed circuit boards. Ajinomoto Build-up Film® (ABF) is the most world-wide used insulating build-up material for manufacturing IC package substrates due to their good resin flow, insulation reliability, thickness uniformity, and Semi-Additive Process (SAP) compatibility. As the recent growth of Fan-Out (FO) type packaging technology driven by its cost advantage and integration benefit, we developed nano-sized filler loaded ABF (Nano filler ABF) as a redistribution layer material. Using Nano filler ABF, we demonstrated 2um/2um line and space Cu patterning and fine via interlayer connection. Our materials with low insertion loss will be introduced due to their advantage for 5G/6G packaging requirement.

Advanced Packaging Opportunities for Small & Mid-Size FPGAs for Various Compute Applications
Raghu (Raghunandan) Chaware, Lattice Semiconductor

Abstract to come

SMT (surface mount technology) reflow observations using standard x-ray and microscopy techniques. One case study incorporates a QFN board layout with vias incorporated in the center thermal pad with solder mask tenting on the back of the board. In another configuration vias were removed from the center thermal pad and vacuum reflow performed with an explanation of why some of the voids can’t be removed. The first and second order results presented within this paper have practical implications and culminated in the development of a novel process evaluation technique coined as Freeze Frame Reflow (FFR). In addition, another case study using an advanced mrQFN (multi-row QFN) package was evaluated using FFR to demonstrate the increase in yield impact this technique can offer.

Novel Filler Technology Study for High Thermal and High Reliability Non-Electrically Conductive Die Attach Paste Adhesive
Xuan Hong, Henkel

Major market demands and packaging trends are driving the continued miniaturization, high functionality and heterogeneous integration systems for semiconductor devices. To make these new designs feasible in application, they are expected to deliver robust thermal management with good heat dissipation, increased performance and higher reliability. Die attach paste adhesives are used to bond electrically active die to metal or composite substrates. In this presentation, the novel filler technology including filler loading, particle size and surface treatment were studied for high thermal conductive electrically insulating die attach paste application to achieve high reliability, such as automotive application. This advanced product offers more capability and flexibility for package design in electronic application.

continued
Wearables/Medical

SiP market and technology trends for wearables applications
Santosh Kumar, Yole

The demand for SiP (system in package) has increased significantly in recent years, with an adoption in a wide ranging of applications. SiP market is expected to increase from $14B in 2020 to more than $198 in 2026. Wearables have emerged as one of the key applications, where SiP approach leads to drastic footprint reduction, improved performance, and functional integration along with EMI isolation and design flexibilities compared to the stand-alone discrete packages at a lower cost. As an example, Apple Watch SiP approach of having double side molding technology for the PMIC has enabled the package footprint of the component with passives to shrink by 37%. Furthermore, the passives are hence placed closer to the PMIC for better performances. The presentation will focus on the market and technology trends of SiP for the wearable applications.

Bio-sensing and its Integration in Wearables
Henry Lin, ASE Group

In the era after Covid 19, people’s awareness toward health care and the demands of remote bio monitoring from medical devices are also rising high. The consumer wearables carry more and more bio sensing functions with huge potential within a limited and constrained space. However, these products are yet reaching customers’ satisfaction and called for more improvements. These improvements are challenging and demanding heterogeneous integration of today’s technologies. The presentation addresses how customer requirements, such as size, comfort, attachment, are considered for the next generation consumer wearables. And most importantly, the requirements can be best achieved by leveraging semi-conductor packaging technologies, in which system miniaturization and sensor integration are among the key topics. SiP, System in Package, and FHE, Flexible Hybrid Electronic, shall be the candidate solutions of heterogeneous integration for wearable products. The presentation will review the status now and explore the future of SiP and FHE applied to the bio sensing application in wearables.

Applying Silicon Photonics to Health Sensor Technology
Dave McCann, Rockley Photonics

Silicon photonics has enabled bringing high speed data over fiber to switch servers in Datacom applications. Integrated silicon photonics is used to transition photons to electrons and back again from electrons to photons. Assembly technologies have been developed to enable these “optical engines”. Rockley Photonics is now applying this technology to health sensors for consumer wearables. An overview of the technology and key assembly capabilities required will be presented.

SiP EDA/Design/Modeling Strategies for 2.xD and 3D Integration
Javi DeLaCruz, ARM

In wireless communication emerging 5G mmWave frequencies are projected to support enormous bandwidth with 1-100ps data speeds. Active research is ongoing to increase the data speeds even more by moving to higher frequencies in the sub-THz frequency range namely, 6G. With a broad range of frequencies to support, advanced packaging solutions are required. This presentation addresses the needs for 5G and 6G communication along with a review of the start of the art for package level integration. The progress made on glass interposer-based solutions at Georgia Tech’s Packaging Research Center will be discussed along with future needs as we progress towards sub-THz frequencies.

Design Flow Challenges for Silicon-centric Multi-chip(let) Packages
John Park, Cadence

High-costs, reticle size limitations and several other factors associated with monolithic system-on-a-chip (SoC) design, are driving companies to look at alternative solutions. For the most part, these companies are now pivoting to multi-chip(let) packaging architectures. A big reason for this shift is that the latest silicon-centric packaging solutions can achieve very similar power, performance, and area (PPA) as a monolithic SoC, while providing a lower-cost more flexible design solution. However, these silicon-centric, cutting-edge multi-chip(let) packaging architectures pose many new design and analysis challenges to both the SoC designers, as well as the package substrate design community. This presentation will cover the current trends in SiP/multi-chiplet packaging architectures and discuss the design and analysis challenges associated with these new technologies.

Ansys: Solving the Unsolvable
Kevin Quillen, ANSYS

Since 1990, Ansys HFSS has been the gold standard for high frequency simulations in the antenna RF world and the signal and power integrity realms. As designs have become more and more challenging, Ansys has continued to expand functionality in the simulation software to increase the size, speed, and ease of use for simulating today’s complex designs. This talk will showcase the many advances Ansys has added to increase the simulation speed, memory sizes, and meshing technologies for SiP packages and PCBs making it possible to solve designs that even a year ago were considered unsolvable.
**On-Demand Sessions**

### HPC/SiPh, Chiplet Integration

#### Packaging Challenges and Opportunities for mmWave Communications

**Dr. Madhavan Swaminathan, Georgia Tech**

In wireless communication emerging 5G mmWave frequencies are projected to support enormous bandwidth with 1-10Gbps data speeds. Active research is ongoing to increase the data speeds even more by moving to higher frequencies in the sub-THz frequency range namely, 6G. With a broad range of frequencies to support, advanced packaging solutions are required.

This presentation addresses the needs for 5G and 6G communication along with a review of the start of the art for package level integration. The progress made on glass interposer-based solutions at Georgia Tech's Packaging Research Center will be discussed along with future needs as we progress towards sub-THz frequencies.

### Facebook Data Centers Heterogenous Integration Driven by AI/ML and Network Applications

**Ravi Agarwal, Facebook**

Talk will focus on system level optimization related to AI/ML and network connectivity, and discuss implication of heterogenous integration in Facebook Data centers. We will also share some of the advanced packaging initiatives FB is participating in as part of Open Domain Specific Architecture (ODSA), an Open Compute Project (OCP) workstream.

### Advanced Die Attach Technologies for the Chiplet Era

**Chris Scanlan, Besi**

Advanced electronic systems are rapidly adopting heterogeneous integration (HI) technologies that utilize multiple chiplets rather than monolithic SoCs. Chiplets are sub-system chips that are connected using standardized, high-bandwidth, low latency interfaces. Chiplet interfaces require very fine pitch interconnects between the chiplet die and the interposer substrate, or interconnect fabric, often a Si interposer or a functional 3D IC. This high-density subassembly may need to be further assembled into a robust finished package. The resulting systems often employ multiple advanced interconnect technologies within the same module. This presentation will review the application of advanced bonding methods used to create complex and highly integrated HI systems based on chiplets. The application of TCB in the assembly of 3D IC and chiplet modules will be reviewed. Advances in hybrid bonding will be discussed, including trade-offs between die to wafer and collective bonding methods.

### SiP Test & Yield Enablement

#### SIP Test Solution for 5G/IoT

**Vineet Pancholi, Amkor Technology**

This presentation will provide a brief description of example SiP designs to alleviate identified concerns. It will then address outsourced semiconductor assembly and test (OSAT) supplier test challenges and solutions being offered today for 5G wireless and Internet of Things (IoT) applications.

### Minimizing deleterious radiation effects in sensitive CMOS devices while maintaining 100% coverage strategies for X-ray defect inspection in double-sided SiP manufacturing

**Francisco Machuca, SVXR**

Thinner packages with more devices, more I/O pins, and more functionality fuel the growth in advanced system-in-package (SiP). And overall, packaged electronic assemblies will extend Moore’s law by disaggregating functions and critically adding memory bandwidth to improve functionality. These advances to SiP and continued dimensional shrinks will also lead to critical changes in the capabilities of the process monitoring or control equipment that supports these developments, including bringing online metro RDA (real-time defect analysis) tools commonplace in front-end processing but lacking in back-end packaging. This report is the successful insertion of the X200™ high-resolution automated X-ray inspection (HR-AXI) tool used to detect manufacturing defects in complex double-sided SiP. The performance benchmarks at a tier 1 OSAT are reviewed, and value gained by the customer will be reported. Additionally, the optimization between safe X-ray dose, speed, and resolution considerations will be described and the production metrics to simplify the qualification for CMOS devices sensitive to ionizing radiation.

### Overview of Warpage and Void Simulations for System in Package (SIP)

**Eric Ouyang, JCET**

System-in-Package (SiP) technology has been used for a wide range of electronic devices, but the void and warpage behavior of the package can be difficult to control and predict due to complex manufacturing parameters and processes. In this presentation, the void and warpage of the SiP strip, as a function of different manufacturing processes, were studied theoretically and experimentally. We will also compare compression molding with transfer molding using a numerical scheme, in the fields of temperature, pressure, flow patterns, and curing kinetics. The presentation will discuss the pros and cons of these two different manufacturing processes.
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