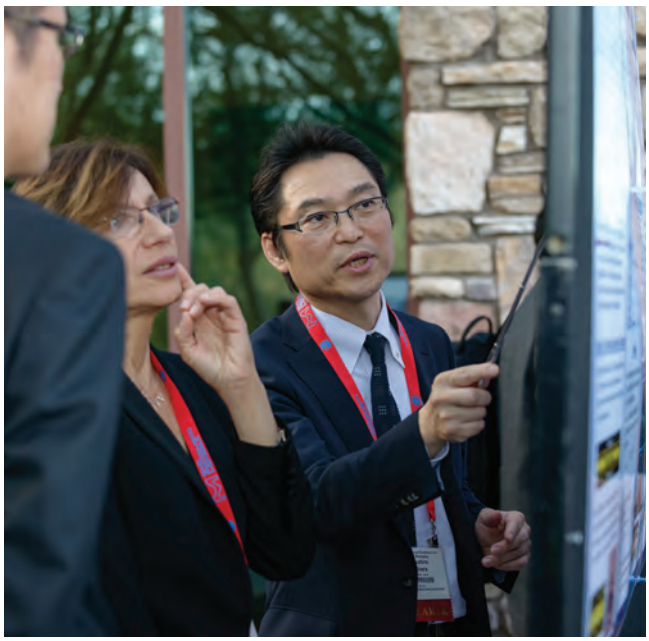
FINAL PROGRAM & EXHIBIT DIRECTORY



14th International Conference and Exhibition on

DEVICE PACKAGING

MARCH 5-8, 2018
We-Ko-Pa Resort | Fountain Hills, Arizona USA
www.imaps.org/devicepackaging

Platinum Premier Sponsor:

ASE GROUP

Gold Premier Sponsors:

EMD Performance Materials

XYZTEC

Silver Premier Sponsors:

Amkor Technology®

NAMICS

Mentor® A Siemens Business

cadence®

KYOCERA

MONDAY, MARCH 5:
13 Professional Development Courses (PDCs)
Welcome Reception: 5:30pm-7:30pm
TUESDAY, MARCH 6-THURSDAY, MARCH 8:
4 Keynotes - 2 Tuesday and 2 Thursday Morning
GBC Plenary Session & Keynote Wednesday
Panel Discussion (Tues.) & Poster Session (Wed.)
Exhibits: 10am-630pm (Tues.), 10am-4pm (Wed.)

ASE GROUP

The SiP Company

USI®

Innovative IC, SiP, and MEMS packaging portfolio to serve dynamic mobility, IoT, high performance computing, and automotive markets.

PoP • Flip Chip • SiP • WLP • Fanout • FOCoS
2.5D • TSV • Flex • AoP • AiP • Shielding
Wire Bond • Embedded • Substrate • Co-Design

Package it.

@asegroup_global

aseglobal.com

IMAPS DPC 2018

Peter Ramm
Fraunhofer EMFT
DPC 2018
General Chair

The IMAPS Device Packaging Conference (DPC) is absolutely one of the premier annual conferences where the latest in microelectronics system integration and packaging technology is unveiled. The 14th DPC will be held in Fountain Hills, Arizona, March 5-8, 2018. The conference, organized by the International Microelectronics Assembly and Packaging Society (IMAPS), provides the stage to showcase the best in packaging technology available today as well as those technologies soon to be released to the market. It offers the benefit of technical exchange among key international players and the opportunity to discover emerging business trends from top marketing analysts.

The conference provides a focused forum on the latest technological developments in three topical workshop tracks related to microelectronic packaging:

Interposers, 3D IC & Packaging; Fan-Out, Wafer Level Packaging & Flip Chip; and Engineered Microsystems and Devices (including MEMS and Sensors).

The 2018 conference will feature four premier Keynote speakers, a Global Business Council (GBC) Keynote and plenary session on the AUTOMOTIVE SYSTEMS DRIVING NEW MICROELECTRONICS OPPORTUNITIES on Wednesday morning, 12 technical sessions featuring more than 75 technical presentations, a poster session & Happy Hour, 13 professional development courses (Monday), a sold-out vendor exhibition and technology showcase, networking receptions and gatherings throughout the week, including: the welcome reception (Monday); the exhibit hall reception (Tuesday); the Poster Session and “Happy Hour” (Wednesday), and a charity golf outing (Thursday), and more - all covering the latest in packaging technology innovation.

We are very excited about the program we put together this year. Since the 3D Integration activities in the industry are growing, we will continue with the same tradition from the past years, having 3DIC being the main subject along other great topics and themes of interest. A dedicated Keynote on 3DIC developments and future trends will be presented by Philip Garrou, Microelectronic Consultant of NC. 3D integration and interposer technologies are today well-accepted approaches for fabrication of high-performance memory-enhanced products, i.e., stacked DRAMs are in high volume production at Samsung, Hynix and Micron, while memory-on-logic stacks are shortly before introduction. On top of the above developments, industrial consortia have been targeting on 3D integration as a key technology for heterogeneous products. In consequence, we chose as hot topic of the DPC 2018 the HETEROGENEOUS INTEGRATION technology, developed for functional diversification systems, as e.g. integration of CMOS with other devices, such as RF components, and sensors. Corresponding Keynotes will be presented by Rozalia Beica from Dow Electronic Materials and by Raja Swaminathan from Intel Corporation, discussing the scope on 2D to 3D packaging architectures in the heterogeneous integration roadmap (HIR) initiative.

We hope you find great value in DPC 2018 this week in Arizona. Be sure to take it all in - visit sessions, attend keynotes, speak with all of the exhibitors, and NETWORK as much as you can! Please visit www.imaps.org/devicepackaging for more updates, and contact the IMAPS staff at the registration desk or any conference organizers if you need any assistance.

EMD
Performance
Materials

EMD Performance Materials is a business of Merck KGaA, Darmstadt, Germany

www.emdgroup.com/en

Program at a Glance

Monday, March 5:

Registration: 7:00 am - 7:00 pm
Professional Development Courses (PDCs): 10:00 am - 5:30 pm
WELCOME RECEPTION: 5:30 pm - 7:30 pm

MORNING Professional Development Courses (PDCs) – 10:00am-12:00pm				
PDC1: Stencil Printing Technology for Bumping and Advanced Semiconductor Assembly Applications ***PDC CANCELLED***	PDC2: Polymer Challenges in 2.5D and 3D Packaging Course Leaders: Jeffrey Gotro, InnoCentrix, LLC	PDC3: The Science of Bond Testing Course Leader: Bob Sykes, XYZTECbv	PDC4: Temporary Bonding of Electronics (Wafers, Packages, Displays) Course Leader: John Moore, Daetec LLC	PDC5: Introduction to System in Package (SiP) - The Heterogeneous Integration Driver Course Leader: Mark Gerber, ASE US
LUNCH *Only provided for those attendees registered for BOTH Morning and Afternoon PDCs*				
EARLY AFTERNOON Professional Development Courses (PDCs) – 1:00pm-3:00pm				
PDC6: Emerging Challenges in Semiconductor Packaging – Part 1 (Design) Course Leader: Raja Swaminathan, Intel	PDC7: Fundamentals of 3D and 2.5D Packaging Integration Course Leader: Urmi Ray, STATS ChipPAC	PDC8: The Evolution of High Density Packaging Course Leader: Phil Garrou, Microelectronic Consultants of NC	PDC9: Introduction to Solder Flip Chip with an Emphasis on Cu Pillar Course Leader: Mark Gerber, ASE US	
COFFEE BREAK IN FOYER				
LATE AFTERNOON Professional Development Courses (PDCs) – 3:30pm-5:30pm				
PDC10: Emerging Challenges in Semiconductor Packaging – Part 2 (Manufacturing) Course Leader: Raja Swaminathan, Intel	PDC11: Manufacturing Failure Analysis and Test Strategies for TSV 3D Packages Course Leader: Bruce Kim, City University of New York	PDC12: MEMS and nanoMEMS Packaging Course Leader: Slobodan Petrovic, Oregon Institute of Technology	PDC13: Fan Out Packaging Evolution & Complexity Course Leader: John Hunt, ASE US	

Tuesday, March 6

7:00 am - 7:00 pm
Registration

8:00 am - 9:55 am
Opening & Keynote Presentations

10:00 am - 6:30 pm
Exhibits Open

10:30 am - 12:30 pm
Technical Sessions - TA1-TA3

12:30 pm - 2:00 pm
Lunch Break In Exhibit Hall

2:00 pm - 5:30 pm
Technical Sessions - TP1-TP3

5:30 pm - 6:30 pm
Reception In Exhibit Hall

6:30 pm - 8:00 pm
Evening Panel Session on:
ADVANCED PACKAGING - WHAT'S NEW? WHAT'S MISSING? WHAT'S NEXT?

Wednesday, March 7

7:00 am - 6:00 pm
Registration

8:00 am - 12:00 pm
GBC Keynote & Plenary Session on
AUTOMOTIVE SYSTEMS DRIVING NEW MICROELECTRONICS OPPORTUNITIES

10:00 am - 4:00 pm
Exhibits Open

12:00 pm - 1:30 pm
Lunch Break In Exhibit Hall

1:30 pm - 5:30 pm
Technical Sessions - WP1-WP3

5:30 pm - 6:30 pm
Poster Session & "Happy Hour"
Outside on Patio/Grass

6:30 pm - 8:00 pm
2018 3D InCites Awards Ceremony
Hosted by IMAPS

Thursday, March 8

7:00 am - 11:30 am
Registration

8:00 am - 9:30 am
Keynote Presentations

9:45 am - 11:45 am
Technical Sessions - THA1-THA3

11:45 am
Conference Ends

1:00 pm - 7:00 pm
IMAPS David Virissimo Memorial Charity Golf Outing

Separate Registration - See Website or contact IMAPS Staff if you are interested to tee it up for a good cause!
WeKoPa Golf Club
1:00 pm Shotgun Start
"Scramble"

THANK YOU to the Device Packaging Sponsors…

PLATINUM PREMIER SPONSOR

ASE GROUP

GOLD PREMIER SPONSORS

EMD Performance Materials

XYZTEC

SILVER PREMIER SPONSORS

Amkor Technology®

NAMICS

cadence

Mentor® A Siemens Business

KYOCERA

Corporate Sponsors

DOW

TECHNIC

SETNA

SPTS An orbotech Company

NGK SPARK PLUGS | NTK TECHNICAL CERAMICS
NTK TECHNOLOGIES, INC.

evatec process systems

APPLIED MATERIALS® make possible

Additional Event Sponsors

Veeco
Mobile Charging Station &
Poster Session Happy Hour

samtec
Poster Session Happy Hour

INTEVAC
Coffee Breaks (3)

TechSearch INTERNATIONAL
Coffee Break

YES
Yield Engineering Systems, Inc.
Evening Panel & Reception

SIP
A New York State Center of Excellence
BINGHAMTON UNIVERSITY
Coffee Break

Kulicke & Soffa
Technology . Innovation . Solutions
Bag Inserts & Web

Official Media Sponsors

3DInCites

ELECTRONICS PROTECTION

Device Packaging Exhibition and Technology Showcase

Exhibiting Companies

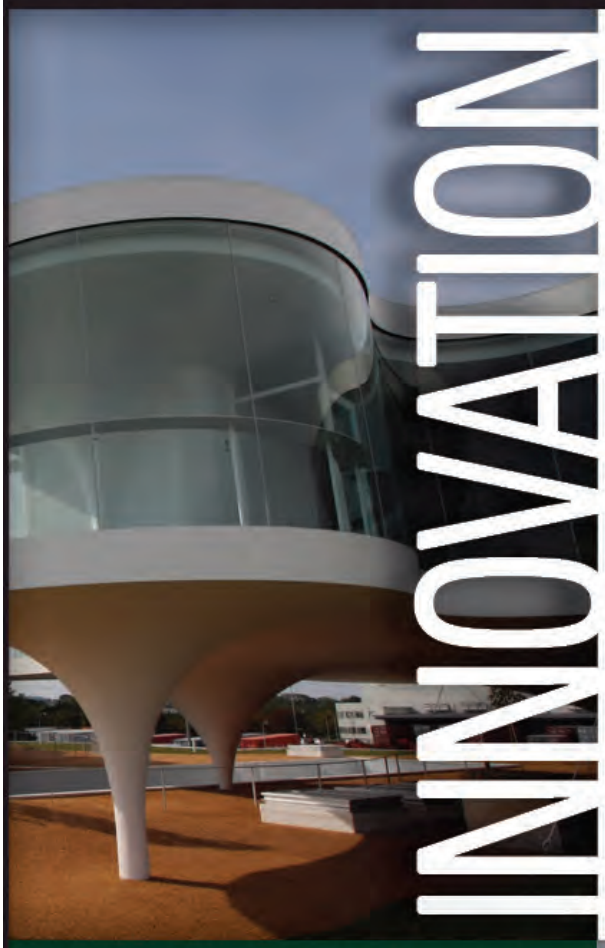
The exhibit hall is now ***SOLD OUT, marking this the 13th consecutive year of a sellout – this year it sold earlier than ever (SEPTEMBER!), and with more than 15 companies on a waitlist!*** The following booths will be on display during Device Packaging 2018. Please visit the companies' websites listed below for more information. The floor plan of the exhibit hall is included on the following page as well. If you have questions about exhibiting with IMAPS, or about getting signed up for the Device Packaging Conference Exhibitions, contact Brian Schieman at bschieman@imaps.org

EXHIBITOR	Booth #
AdTech	12
AGC	34
AI Technology	66
AMICRA Microtechnologies	26
Amkor Technology, Inc.	37
ASE Group	47
ASM Pacific Technology	55
AT&S America	24
ATV Technologie GmbH	13
Axus Technology	22
Boschman Technologies / APC	2
Cadence Design Systems, Inc.	43
Chalman Technologies	8+9
DeWeyl Tool Company	17
Dow Electronic Materials	19
EMD Performance Materials	38
EV Group, Inc.	41
Evatec	49
F&K Delvotec, Inc.	59
FlipChip - Huatian	18
Hesse Mechatronics, Inc.	7
HSIO Technologies	5
IBM Canada Ltd.	16
IMAT, Inc.	29
JSR Micro, Inc	6
Kyocera	40
LINTEC of America, Inc.	11
MacDermid Enthone / Alpha Advanced Materials	45+46
Mentor, A Siemens Business	48
Metalor Technologies USA	15
Micro Systems Technologies Management AG	28
MicroChem Corp.	58
Microconnex	3
Micross	52
Mini-Systems, Inc.	4

EXHIBITOR	Booth #
NAMICS	39
nanosystec Inc.	10
Neutronix-Quintel	53
Nikon Precision Inc	51
NTK Technologies	21
PacTech USA Inc.	56
Palomar Technologies	63
Plasma-Therm, LLC	65
Rudolph Technologies, Inc.	32
SETNA	50
SHINKO Electric America, Inc.	44
Sikama International Inc	35
SMART Microsystems Ltd	14
Sonoscan, Inc.	33
SPTS	42
Sputtering Components Inc	30
STATS ChipPAC	23
StratEdge Corporation	62
Superior Silica	31
Technic	25
TechSearch International	20
Teikoku Taping System, Inc.	57
Unisem	1
UnitySC	60
XYZTEC	61
Yield Engineering Systems	64
Yole Developpement	36
Yxlon FeinFocus	54
Zuken, Inc	27

It's why NAMICS® thrives inside every gadget and outside every box.

#1 PIONEER OF CONDUCTIVE & INSULATION MATERIALS FOR ELECTRONICS



Founded in 1946, NAMICS® offers a diverse portfolio of award-winning conductive, insulation and film materials for electronics. Our global distribution network, peerless R&D commitment, and superior customer service rank us as the world leader in our industry.

- AWARD-WINNING TECHNOLOGY
- REVOLUTIONARY R & D FACILITIES
- SUPERIOR CUSTOMER SERVICE
- GLOBAL DISTRIBUTION NETWORK
- ISO9001 ACCREDITED

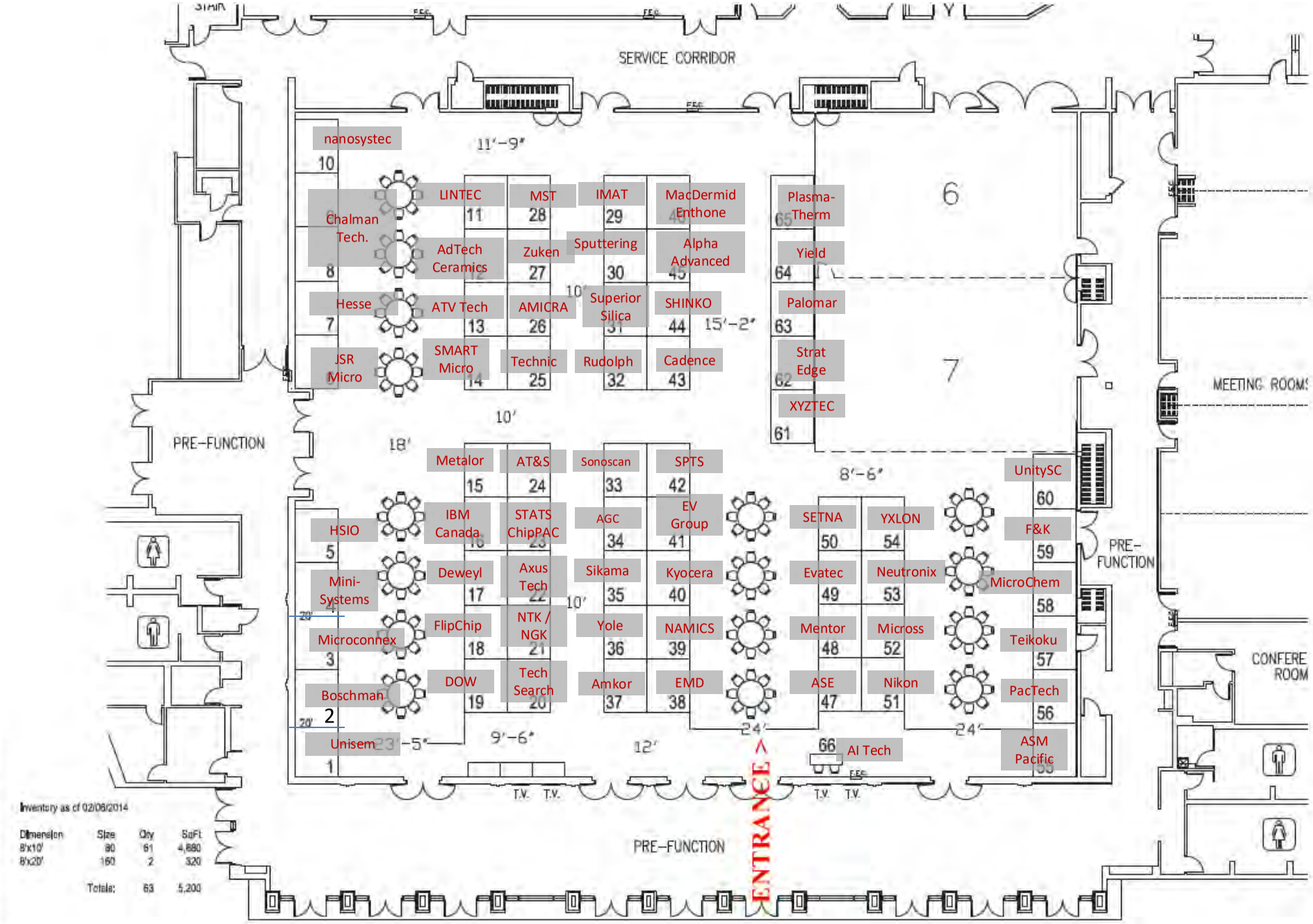
NAMICS CORPORATION

TO LEARN MORE

☎ (408) 516-4611

www.NAMICS.co.jp

DEVICE PACKAGING 2018 – EXHIBIT FLOORPLAN



EXHIBITS DIRECTORY

Please stop by and visit these companies during your time at Device Packaging 2018

THANK YOU EXHIBITORS FOR YOUR SUPPORT!

Booth: 12

AdTech Ceramics

511 Manufacturers Road
Chattanooga, TN 37405
(P) 423-755-5400
(E) sales@adtechceramics.com
www.adtechceramics.com

AdTech Ceramics is a fully integrated US based manufacturer of high temperature co-fire ceramic (HTCC) electronic packages and precision injection molded ceramic components. Standard ceramic materials offered include multilayer aluminum oxide and aluminum nitride. AlN is often preferred due to its excellent thermal conductivity and desirable coefficient of thermal expansion. AdTech also produces chemically or CNC milled metal components including package lids, leads and seal rings. Our injection molded products can be provided as fired, with metallization and plating or as full ceramic-to-metal assemblies. In our continuous drive for innovation and advanced technology for our growing customer base, we have recently added copper thick film metallization on alumina or aluminum nitride and ENEPIG plating capabilities. Located in Chattanooga, TN and with over 45 years of experience producing multilayer ceramic packages, we are ideally positioned to take on your most challenging package designs. Originally established as American Lava in 1903, AdTech has been owned by 3M, GE and Coorstek prior to is becoming Advanced Technical Ceramics Company in 2004. AS9100C/ISO9001:2008 certified.

Booth: 34

AGC Electronics America

18694 Caminito Pasadero
San Diego CA 92128
(P): 714-745-3193
(E): vstygar@agcem.com
www.agcem.com

AGC is a leader of glass, fluorinated polymers and synthetic quartz for the global automotive and electronics device industries. AGC provides specialized formulations of alkali-free alumino-borosilicate glass suitable for LED, MEMS, and interposer electronics substrates. Our high volume capability for glass and value-added services such as drilling vias, AR coatings, and via fill technologies makes AGC a valuable partner for your next generation mobile or Life Science product. AGC's fluorinated polymer is ideally suited for dielectric coatings, or creating micro or nano-sized vias for Lab on a Chip applications in the Life Science technologies sector. AGC's fluorinated polymer is highly transparent to 250 nanometers. It has the ability to change from a hydrophilic to a hydrophobic surface. AGC's fluorinated material is the ideal candidate for passive and active coatings. AGC's premier synthetic quartz with unparalleled formulation controls result in the lowest insertion loss and nearly zero auto fluorescence of any material. This provides our customers the highest electrical performance loss for high frequency circuits. In addition, AGC's synthetic quartz' low auto fluorescence makes it an excellent substrate for photonic applications in Lab on a Chip reactors.

Booth: 66

AI Technology

70 Washington Road
Princeton Junction, NJ 08550
(P) 609-799-9388 ext-124
(E) achauhan@aitechnology.com
www.aitechnology.com

AI Technology, Inc. (AIT) developed flexible epoxies for microelectronic packaging in 1985. Today, AIT's product line includes patented component, substrate and large die bonding adhesives and underfills, stack-chip packaging with dicing die-attach film (DDAF), flip-chip bonding and underfilling, single and multiple-chip module die bonding (230°C and above), and component and substrate bonding adhesives for military and commercial applications. AIT's thermal interface materials, including phase-change pads, greases, gels and adhesives, ensure ultimate performance in semiconductors, modules, computers and communication electronics applications.

Booth: 26

AMICRA Microtechnologies

1250 Oakmead Parkway, Suite 210
Sunnyvale, CA 94085
(P) +49 941 208209 0
(E) sales@amicra.com
www.amicra.com

AMICRA Microtechnologies is a worldwide leading supplier of Die Attach Equipment specializing in submicron placement accuracy (+/- 0.3µm@3sigma). Equipment offering supports Die Attach and Flip Chip bonding processes including the following capability: in-situ eutectic bonding, dynamic alignment, heated tool, pulse heating, laser heating, volumetric and jet dispensing, active bond force control, high speed solutions, in-situ UV curing, 600 x 550mm bonding area, quantitative tilt calibration system, etc. Market focus: PIC/SiPhotonics, Automotive Sensors LiDAR, Optoelectronics, AOC, FanOut. Other products include: High Speed Wafer Inking and inspection, Automated LED/LD Test & Sort Systems, Gel Fill Line and Custom Solutions.

Booth: 37

Amkor Technology, Inc.

2045 E. Innovation Circle
Tempe, AZ 85284
(P) 480-821-5000
(E) sales@amkor.com
www.amkor.com
Twitter: twitter.com/AmkorTechnology

Amkor Technology, Inc. is one of the world's largest and most accomplished providers of semiconductor packaging and test services. Founded in 1968, Amkor pioneered the outsourcing of IC assembly and test and is a strategic manufacturing partner for more than 250 of the world's leading semiconductor companies, foundries and electronics OEMs. Amkor's operational base encompasses more than 10M ft2 of floor space with production facilities, product development centers and sales & support offices located in key electronics manufacturing regions in Asia, Europe and the United States. For more information visit www.amkor.com.

Booth: 47

ASE Group

1255 E. Arques Ave.
Santa Clara, CA 94086
(P): (408) 636-9500 x572
(E): patricia.macleod@aseus.com
www.aseglobal.com
Twitter: @asegroup_global

Alongside a broad portfolio of established technologies, OSAT industry leader ASE is also delivering innovative advanced packaging and System-in-Package solutions to meet growth momentum across a broad range of end markets. For more about our advances in SiP, Fanout, WLP, MEMS, Flip Chip, and, 2.5D, 3D & TSV technologies, all ultimately geared towards applications to improve lifestyle and efficiency, please visit: www.aseglobal.com

Booth: 55

ASM Pacific Technology

7850 South Hardy Dr. Suite 110
Tempe, AZ 85284
(P): 602-437-4892
(E): Bud.Troche@asmpt.com
http://www.asmpacific.com/asmpt/index.htm

ASM Pacific Assembly Products is a Sales and Marketing Division of ASM Pacific Technology (ASMPT). ASMPT is the world's leader in back end Assembly and Microelectronic Equipment. With a vision of providing cost effective complete factory automation solutions to our customers for their Assembly and Packaging needs. ASMPT also is an industry leader in Lead frame manufacturing technology that is in the forefront of the Semiconductor Industry.

Booth: 24

AT&S

1735 N. First Street, #245
San Jose, CA. 95124
(P) 408-573-1211
(E) s.clifford@ats.net
www.ats.net

AT&S is a leading HDI, flex circuit, and IC substrate producer offering Embedded Component Packaging (ECP®) technology for embedding passives and bare ICs inside the laminate for IC packages and printed circuit boards. Embedding provides increased component density and smaller body size; improved signal integrity with embedded capacitors located just microns directly below the IC; thermal management with filled copper vias directly on the die backside; improved shock & drop robustness; and hidden components for security and reverse engineering resistance. Additional components can be mounted on the top and bottom surfaces and connected to the embedded components by copper-plated laser micro-vias. AT&S has six manufacturing sites in Austria (2), China (2), India, and South Korea. Embedding is available in the Leoben (Austria) factory and the Shanghai (China) factory. FC-BGA substrates are produced in the Chongqing (China) factory. Flex and rigid-flex circuits are produced in the Ansan, South Korea factory. AT&S has local offices in San Jose and Chicago, and throughout Asia in Japan, Korea, Taiwan, China, and Hong Kong. AT&S: The First Choice for Advanced Applications.

Booth: 13

ATV Technologie GmbH

Johann-Sebastian-Bach-Strasse 38
Vaterstetten 85591 Germany
(P) 0049-8106-3050-23
(E) sales@atv-tech.de
www.atv-tech.de

Founded in 1982 ATV Technologie GmbH is an international player in the field of micro electronics focussing on manufacturing and distribution of vacuum soldering devices and processing ovens. With an expert team of engineers and physicists rooted in precision mechanics, eletronical and mechanical engineering ATV Technologie GmbH designs and develops a product range at the highest level of quality. ATV offers long-standing experience in designing and manufacturing high-end process stoves featuring precise temperature control and excellent homogeneity for semiconductor technology and micro electronics as well as a worldwide network of special representatives who will take care of on-site sales and service.

Booth: 22

Axus Technology

7001 W. Erie St. Suite 1
Chandler, AZ 85226
(P) 480-705-8000
(E) info@axustech.com
www.axustech.com

Axus Technology provides surface processing solutions for a range of semiconductor, MEMS, substrate, and related technologies. With a highly experienced engineering team, Axus Technology applies proven process technology to the production and development of CMP processes, advanced substrate development, and advanced packaging applications including 3-D integration and through-silicon-via processes. Along with providing support services for existing tools, Axus Technology delivers economical leading-edge equipment and process solutions that are precisely configured for end-user applications. Based in Chandler, Arizona, Axus Technology operations include a fully-equipped development and CMP foundry processing facility, as well as design, manufacture, and worldwide service operations. For more information visit our website at www.AxusTech.com.

Booth: 2

Boschman Technologies / APC

Stenograaf 3
Duiven, Netherlands 6921EX
(P) 480-488-9898
(E) john@jhcrane.net
www.boschman.nl & www.apcenter.nl

Boschman Technologies is the world leading supplier of automatic molding systems and sintering systems. Film is used for the encapsulation of Sensor and MEMS devices. This process, called Film Assisted Molding is ideal for applications where sensing surfaces or bond pads or heat sinks must be exposed and free of mold compound bleed and flash. This technology is used for MEMS, Sensor, Solar, and Optical molding applications with the transfer molding of epoxy or silicone based mold compounds, including clear materials. Automatic sintering systems are used for pressure assisted nano-silver sintering for die, clip and heat sink attach. APC, Advanced Packaging Center, serves as a one-stop shop for research, development, qualification, prototyping and small volume manufacturing services by focusing on MEMS, Sensors, and advanced IC, wafer level packaging, power package and rf package applications for molding and sintering.. By working closely with customer R&D departments to explore new packaging concepts, value from Innovation to Industrialization is provided.

Booth: 43

Cadence Design Systems

2655 Seely Ave.
San Jose, CA 95134
(P) 408-914-1234
(E) events@cadence.com
www.cadence.com
Twitter: https://twitter.com/cadence

Cadence enables electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work and play. Cadence® software, hardware and semiconductor IP are used by customers to deliver products to market faster. The company's System Design Enablement strategy helps customers develop differentiated products—from chips to boards to systems—in mobile, consumer, cloud datacenter, automotive, aerospace, IoT, industrial and other market segments. Cadence is listed as one of Fortune Magazine's 100 Best Companies to Work For. Learn more at cadence.com.

Booth: 8+9

Chalman Technologies

3150 E. La Palma Avenue, Suite K
Anaheim, CA 92806
(P): 714-632-1724
(E): keith@cti-rep.com
www.cti-rep.com

Chalman Technologies, Inc. (CTI) is an engineering oriented manufacturers' representative organization experienced in semiconductor, fiber optic, and other microelectronics technologies. We specialize in materials and equipment for these industries, including assembly, rework, & test equipment as well as materials for electronic assembly. In addition, we also provide HEPA filters, laminar flow workbenches and other equipment to meet your cleanroom requirements.

Booth: 17

DeWeyl Tool Company

959 Transport Way
Petaluma, CA 94954
(P) 707-765-5779
(E) david.p@deweyl.com
www.deweyl.com

DeWeyl provides the finest quality bonding wedges in the world. Located in the Petaluma, CA, DeWeyl's primary business is manufacturing wire bond wedges and custom high precision tooling for the semiconductor, aerospace and medical industry. DeWeyl produces wedges made from ceramic, titanium and tungsten carbide for small and large round wire and ribbon applications.

Booth: 19

Dow Electronic Materials

455 Forest Street
Marlborough, MA 01752
(P) 508-481-5970
(E) markowski@dow.com
www.dowelectronicmaterials.com

Dow Electronic Materials, a global supplier of materials and technologies to the electronics industry, brings innovative leadership to the semiconductor, circuit board, finishing, display, photovoltaic, and LED markets. From advanced technology centers worldwide, teams of talented Dow research scientists and application experts work closely with customers, providing solutions, products and technical service necessary for next-generation electronics. Dow's portfolio includes metallization, dielectric, lithography and assembly materials designed to meet the most demanding needs for advanced semiconductor packaging applications, such as bumping, copper pillars and redistribution layer (RDL), passivation, underbump metallization (UBM), thermal interface and lid seal adhesion used for the latest fan-out wafer level packaging (FOWLP), flip chip, system in package (SiP), and 2.5D/3D chip packages.

Booth: 38

EMD Performance Materials

6555 Nancy Ridge Drive, #200
San Diego CA 92121
(P) 858-883-3473
(E) james.haley@emdgroup.com
www.emd-performance-materials.com/en/index.html

Performance Materials comprises the entire specialty chemicals business of Merck KGaA, Darmstadt, Germany. The portfolio includes high-tech performance chemicals for applications in fields such as:

- Displays
- Integrated Circuits
- Lighting Applications
- Solar & Energy
- Coatings
- Semiconductor Packaging

Customer sectors in consumer electronics, lighting, printing technology, plastics applications and integrated circuits make use of materials and solutions from EMD Performance Materials. Thanks to comprehensive investments in research & development, we are constantly extending our leading position as an innovator and reliable partner.Our future growth integrates key materials consisting of high purity chemicals used in wafer fabrication to sustainable materials for advanced back end solutions.

Booth: 41

EV Group

7700 S River Parkway
Tempe, AZ 85284
(P) 480-305-2400
(E) salesnorthamerica@evgroup.com
www.evgroup.com

EV Group (EVG) is a leading supplier of equipment and process solutions for the manufacture of semiconductors, microelectromechanical systems (MEMS), compound semiconductors, power devices, and nanotechnology devices. Key products include wafer bonding, thin-wafer processing, lithography/nanoimprint lithography (NIL) and metrology equipment, as well as photoresist coaters, cleaners and inspection systems. Founded in 1980, EV Group services and supports an elaborate network of global customers and partners all over the world. More information about EVG is available at www.EVGroup.com.

Booth: 49

Evatec

780 Carillon Parkway, Suite 150
St Petersburg, Florida, 33716
(P): 727-201-4313
(E): infoNA@evatecnet.com
www.evatecnet.com

From 5G mobile network solutions and the new generation of intelligent HB LED based lighting in our automobiles, to Gesture Recognition Capability and EMI shielding for our smart phones, our thin film deposition systems enable manufacture of the worlds highest performance, semiconductor, optoelectronic and optical devices. Our Advanced Process Control (APC) technologies enables new levels of production yields for some of the most challenging thin film performance specifications . We provide hardware and process know how to our customers in Advanced Packaging, Power Devices, MEMS, Wireless Communication , Optoelectronics and High Precision Optics using a range of batch, cluster and inline tools according to their process and throughput requirements. Within Advanced Packaging our production solutions on HEXAGON and CLUSTERLINE deliver high yield UBM / RDL processes with stable low Rc values at throughputs up to 56 wafers per hour in FOWLP. Combining our latest batch degas, etch and deposition technologies enables our customers to achieve the even lower Rc values needed for contacts and interconnects required next generation power management in IOT applications.

Booth: 59

F&K Delvotec

27182 Burbank
Foothill Ranch, CA 92610
(P) 949-595-2200
(E) dominic.sha@fkdelvotecusa.com
www.fkdelvotec.com/en

F&K Delvotec is the worldwide leader in innovative wire bonding technology. F&K Delvotec's expansive portfolio of products deliver intelligent one-stop shop solutions for any wire bonding application, from lab bond process development to completely automated systems. Over 40 patents in wire bonding technology, and award-winning new products and customer satisfaction, attest to the continuing emphasis on providing innovative solutions that drive the industry forward. Whatever bonding is required, F&K Delvotec delivers smart technology that follows the "staying ahead" philosophy that is the heart of the company. F&K's main office is in Germany, with satellite offices in Singapore and the U.S. For more information, please visit www.fkdelvotec.com/en.

Booth: 18

FlipChip - Huatian

3701 E. University Dr.
Phoenix, AZ 85034
(P): 602-431-6020
(E): anthony.curtis@flipchip.com
www.flipchip.com

FCI-HT supplies turnkey semiconductor assembly and test services to the consumer, automotive, industrial and medical industries. FCI-HT supports a wide range of customers, frequently partnering with them to engineer customized solutions including expedite bumping and backend services on Multi-Project Wafers. FCI-HT is a leader in wafer level packaging with patented technologies spanning from Cu Pillar Bumping, Spheron™ Wafer Level Chipscale Packaging, and ChipsetT™ Embedded Die Packaging. FCI-HT is a division of Huatian Technologies (HT). HT is among the top 6 OSATs in the world with over one billion dollars in annual revenue. It is listed on the Shenzhen Stock Exchange Market. Huatian has six ISO/TS16949 factories located in the US and China offering a complete range of semiconductor packaging and turnkey services.

Booth: 7

Hesse Mechatronics, Inc.

213 Hammond Ave
Fremont, CA 94539
(P): 480-361-5029
(E): jolynn.snell@hesse-mechatronics.us
www.hesse-mechatronics.us

Hesse Mechatronics, Inc. is a wholly-owned subsidiary of Hesse GmbH, one of the world's leading producers of fully automated wedge wire bonders. The main expertise of Hesse GmbH is the development, manufacturing and marketing of fully automated machines for interconnect and assembly technologies, including standard and product-specific automation solutions. Hesse GmbH was founded in 1986.

Booth: 5

HSIO Technologies

13400 64th Ave N
Maple Grove, MN 55311
(P): 763-447-6260
(E): randy.knudsen@hsiotech.com
www.hsiotech.com

HSIO Technologies and HSIO Circuit Technologies mission is to develop new, exciting, and proprietary technology to address high-density and high-speed interconnect challenges faced by our customers and the semiconductor industry.. HSIO is focused on improving the signal channel through the various circuits, connectors and components our customers use to develop, validate and deploy silicon to the market. HSIO's Grypper socket products are unique in that it requires no lid and is the same footprint as the device under test. HSIO Circuit Technologies Flex and Rigid Flex PCB manufacturing featuring < 35 micron lines and spaces and 10 micron feature sizes. The processes enable improved signal integrity, reduced cross-talk, and improved impedance matching by selectively fabricating structures which precisely tune the interconnect device's impedances to those of its operating environment.

Booth: 16

IBM Canada Ltd

23 Airport Blvd
Bromont, Quebec Canada J2L1A3
(P) 450-531-2474
(E) assembly@ca.ibm.com
www.ibm.com/assembly

IBM, located in Bromont Canada, is a world leader in semiconductor packaging technology, products and services. Now available to customers worldwide, we invite you to take advantage of our experience, system level mindset, and skilled engineers to execute your most advanced packaging and test solutions. Tap into our deep competencies as the industry continues to shift to custom SoCs and SiPs. IBM is known for its multi-chip packaging and heterogeneous integration. We offer full turnkey solutions from modelling and characterization through Burn-in and test. Our test capability spans digital, analog, mixed signal, RF as well as multi-site programming, test pattern conversion, and load board design. We provide high quality mechanical, thermal and electrical design (including high speed/SERDES, signal integrity and power integrity), ensuring effective execution of new and updated platforms. Services include materials and process characterization, optimized substrate design, and failure analysis while package platforms range from large organic substrates to silicon and glass interposers, and the newest coreless technologies. We invite you to discuss your next generation requirements – our developments in areas such as silicon photonics are unrivaled. IBM will help you deliver differentiated solutions while providing personalized, expert support to meet even the toughest application goals. Our advanced Flip Chip assembly site is 1A Trusted and ITAR compliant.

Booth: 29

IMAT, Inc.

12516 NE 95th St. Suite D110
Vancouver, WA 98682
(P): 360-256-5600 x16
(E): ericf@imatinc.com
www.imatinc.com

Quality Custom in-house silicon wafer processing. We offer a wide variety of custom films and Services. Processing on 50mm- up to 450mm wafers. Bump / RDL / and TSV patterning. Thick resist patterning. Metal Deposition. Thermal Oxidation. Warped wafer fabrication. Feel free to contact us for quotations: 360-256-5600 ext.16.

Booth: 6

JSR Micro, Inc

1280 N. Mathilda Ave.
Sunnyvale, CA 94089
(P) 408-543-8800
(E) atseng@jsrmicro.com
www.jsrmicro.com

JSR's unique THB series of negative tone thick film photoresists for RDL, micron bump, and Cu pillar applications, along with our WPR series of dielectric coatings are ideal for WL-CSP, Flip Chip, TSV, and other packaging technologies. JSR materials provide excellent throughput, large process margins, high aspect ratio solutions for film thicknesses from <10 to >100 micrometers while being processed in standard TMAH developer. Additionally, JSR offers exceptional materials in the temporary bonding space – contact us to learn more.

Booth: 40

Kyocera

8611 Balboa Ave.
San Diego, CA 92123
(P): 858-576-2600
(E): kaicorp@kyocera.com
americas.kyocera.com/kai-semiparts/

Kyocera International, Inc., Semiconductor Components Group (KII-SC) has been manufacturing ceramic packages in San Diego, CA since 1971. Kyocera offers an extensive array of semiconductor packages and complex modules for simple to challenging applications including RF, millimeter wave, power semiconductor, DNA sequencing, phased array radar, and space / telecom. Packages are available in HTCC, LTCC, MTCC, HiTCE, AlN and BeO. Also available are organic build-up packages, state-of-the-art high-density PCBs, and assembly materials such as Ag sinter paste and high Tc epoxies. Kyocera has state-of-the-art package design capability in-house that includes electrical and thermo-mechanical design, modeling / simulation and analysis to maximize package and circuit performance in your application. Our Assembly Technology Division accepts prototype to volume production orders for flip chip, wirebond, wafer dicing, and vacuum soldering to provide a convenient one-stop-shop solution for customers.

Booth: 11

LINTEC of America, Inc.

15930 S. 48th Street, Suite 110
Phoenix, Arizona 85048-0428
(P) 480-966-0784
(E) Maya-Gordon@lintec-usa.com
www.lintec-usa.com

LINTEC is a worldwide leader in adhesive technologies through the Adwill brand of products. For 30+ years, LINTEC has created equipment and continues to develop materials to solve difficult semiconductor wafer level packaging issues. LINTEC has a catalog of hundreds of tapes, a myriad of equipment, and decades of application experience to help. Whether you are looking for a tape, need equipment to mount, peel, or UV cure, or would like assistance from our applications labs in Phoenix and Dallas to tackle a difficult issue; our staff stands ready to assist you to provide the Adwill Advantage. We are located at booth #11 in the exhibition hall. On display is our 2-in-1 backgrind and bump support material for wafer level packaging.

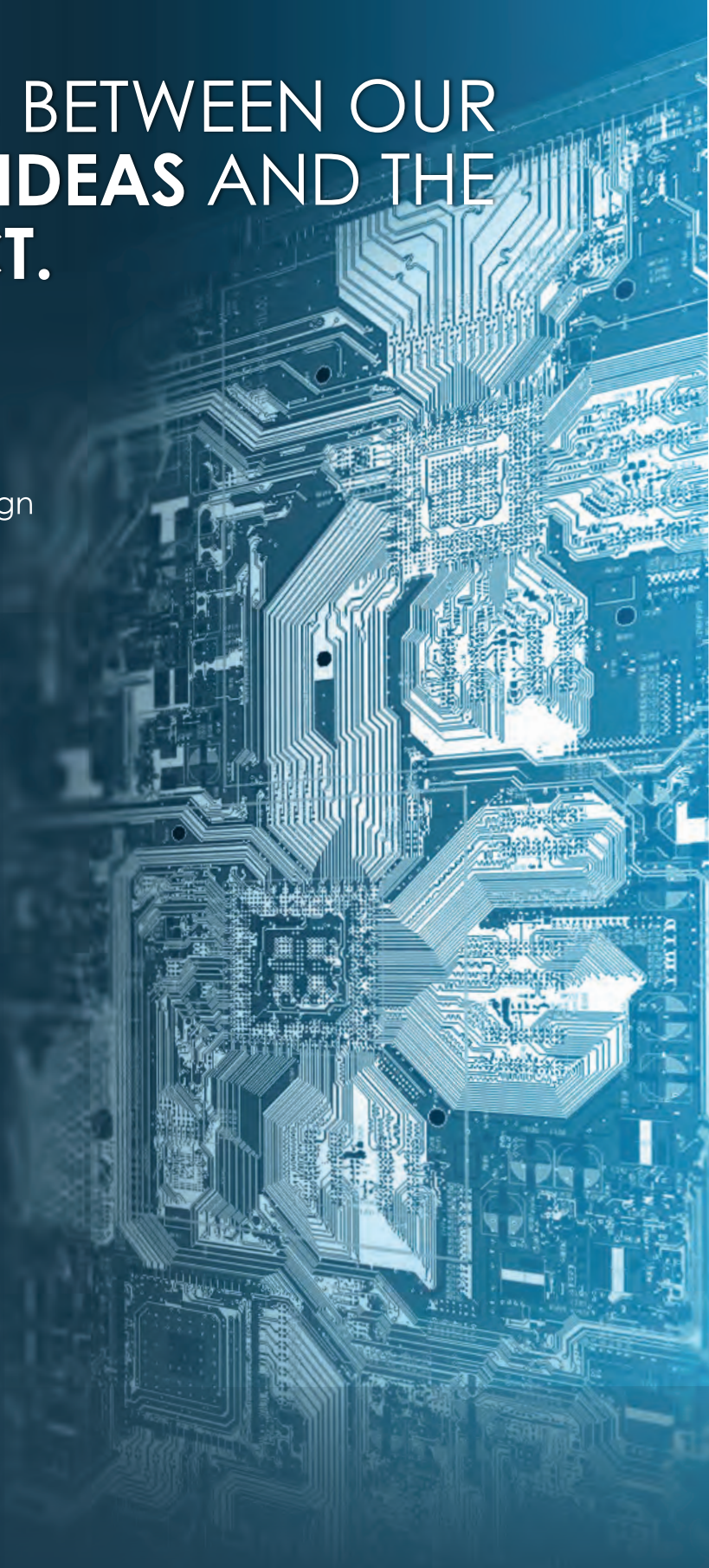
Booth: 45+46

MacDermid Enthone / Alpha Advanced Materials

227 Freight Street
Waterbury, CT 06702
(P) 203-575-5700
(E) info@macdermidenthone.com
www.electronics.macdermidenthone.com

MacDermid Enthone's Advanced Electronics Solutions (AES) business is a global leader in high performance semiconductor chemistries and assembly materials. OEMs, IDMs, wafer foundry engineers, tool suppliers, and OSATs should visit the IMAPS booth to collaboratively develop solutions that meet the fast paced semiconductor market demands. The AES team will highlight the MICROFAB family of products which provides advanced packaging solutions that exceed aggressive packaging design requirements and enable greater device reliability. MEES will showcase its chemical processes for IC substrates, including PackagePrep solderable finish for QFN sidewalls, and PackageBond leadframe adhesion promoter. The booth will also include specialty product offerings from their sister company, Alpha Advanced Materials (AAM). AAM is committed to providing the global semiconductor packaging industry with innovative high performance materials including ATROX, the hybrid sintering die attach paste, and their full suite of solder, spheres and wafer level fluxes. Each technology supports a broad spectrum of package applications that ranges from MEMS, RF filters and PAs to leading edge FOWLPs, high die count memory stacks and high performance RF modules. The combined innovation, experience and product offerings make MacDermid Enthone and Alpha the new industry leader in all materials for Advanced Packaging.

NOTHING STANDS BETWEEN OUR **CUSTOMERS' BEST IDEAS** AND THE **FINISHED PRODUCT.**



Xpedition®
Enterprise PCB & Package Systems Design

PADS®
PCB Product Creation for
Small Teams & Engineers

HyperLynx®
Fast, Accurate, and Comprehensive
Analysis Solutions

Valor® NPI
Lean NPI and DFM

Stop by our booth for more details.

Learn more at:
www.mentor.com/pcb
www.pads.com

Mentor®
A Siemens Business

Booth: 48

Mentor, A Siemens Business

1811 Pike Road
Longmont, CO 80501
(P) 720) 494-1014 x1270
(E) jennifer_chausse@mentor.com

We enable companies to develop better electronic products faster and more cost-effectively. Our innovative products and solutions help engineers conquer design challenges in the increasingly complex worlds of board and chip design.

Booth: 15

Metalor Technologies USA

255 John L Dietsch Blvd
North Attleboro MA 02761
(P): 508-699-8800
(E): michelle.wheeler@metalor.com
www.metalor.com/

Metalor's Advanced Coatings Division is uniquely positioned as the only global source of precious metal commodities and plating solutions with manufacturing sites and refineries throughout US, Asia, and Europe. Our comprehensive plating process range includes precious metal solutions and ancillary products. Metalor offers gold, silver, platinum, palladium, rhodium, ruthenium materials designed for use in semiconductor, electronic, and decorative applications. We offer a complete service; the supply of precious metal replenishment salts and anodes, process chemistry, as well as refining services can be your one-stop provider for precious metal needs. Our Technical Service Team, located facilities worldwide, is on call and equipped to provide rapid response to specific customer queries as well as on-site installation support.

Booth: 28

Micro Systems Technologies, Inc.

6024 SW Jean Road
Lake Oswego, OR 97035
(P) 5037448900
(E) sales.msti@mst.com
www.mst.com

The MST group is specialized in developing and manufacturing miniaturized, integrated electronic module solutions. The capabilities include highly complex HDI/microvia PCBs, semiconductor packaging processes as well as advanced assembly in the field of SMT and chip & wire.

Booth: 58

MicroChem Corp.

200 Flanders Road
Westborough, MA 01581
(P) 423-384-1486
(E) mquillen@microchem.com
www.microchem.com

MicroChem develops and manufactures specialty chemicals including photoresists and ancillary materials for MEMS, Microelectronics, Advanced Lithography, Specialty Displays, Packaging, Optoelectronics and other dynamic technology markets.

Booth: 3

MicroConnex

34935 SE Douglas St.
Snoqualmie WA 98065
(P) 425-396-5707
(E) hello@microconnex.com
www.microconnex.com

MicroConnex = flexible electronics. MicroConnex offers fine-line flex circuits and laser microdrilling/machining. Capabilities include flexible printed circuits; high-density, fine-line, and fine-pitch (less than 2 mil trace/space); prototyping to production; laser-drilled blind, buried, and through-hole microvias; laser micromachining and drilling; and thin-film deposition.

Booth: 52

Micross

7725 North Orange Blossom Trail
Orlando, FL 32810
(P) 407-298-5664
(E) valerie.thomas@micross.com
www.micross.com
@microsscomps

Micross is the leading one-source, one-solution provider of bare die & wafers, wafer bumping & advanced interconnect technologies, custom packaging & assembly, component modification services, electrical & environmental testing and Hi-Rel products to manufacturers and users of semiconductor devices. In business for 35+ years, our comprehensive array of high-reliability capabilities serves the global defense, space, medical, industrial and fabless semiconductor markets. Micross possesses the sourcing, packaging, assembly, test and logistics expertise needed to support an application throughout its entire program cycle. Micross Advanced Interconnect Technology (AIT), a specialized division of Micross, is home to one of the premier wafer bumping and wafer level packaging facilities in the U.S., with 20+ years of experience developing and providing leading edge interconnect and 3D integration technologies (TSV, Si interposers, 3D IC) to customers around the world. AIT has the unique ability to support early stage development needs as well as low-to-mid volume production for more mature applications and platform technologies. Our ITAR-registered facility supports wafer sizes up to 200mm with established and proven processes and the flexibility to tailor unique solutions for your most demanding interconnect requirements. The facility can also support the processing of non-standard materials, as well as the fabrication of novel device structures (e.g. MEMS and 3D microstructures).

Booth: 4

Mini-Systems, Inc.

20 David Rd., P.O. Box 69
N. Attleboro, MA 02761-0069
(P): 508-695-0203 x1305
(E): mtran@mini-systemsinc.com
www.mini-systemsinc.com

For over 44 years, MSI has been supplying superb quality and on-time deliveries. Absolute tolerances starting at 0.005% and TCR's at 2ppm/C. Case sizes start at 0101. Standard deliveries under 2 weeks. MSI is ISO 9001 certified and is on the QPL for MIL-PRF-55342 and MIL_PRF-32159.

Booth: 39

NAMICS Corporation

2055 Gateway Place, Suite 480
San Jose, CA 05110
(P) 408-516-4611
(E) info@namics-usa.com
www.namics.co.jp/e/

NAMICS Corporation is a leading source for underfills, encapsulants, adhesives, and insulating and conductive materials used by producers of semiconductor devices, passive components and solar cells. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea and China, NAMICS serves its worldwide customers with enabling products for leading edge applications.

Booth: 10

nanosystec Inc.

45401 Research Ave, Ste 140A
Fremont, CA 94539
(P) 844-811-8782
(E) sales@nanosystec.com
www.nanosystec.com

Nanosystec provides state-of-the-art alignment and assembly stations for optoelectronics packaging. The stations offer a large degree of automation, high yield and maximum coupling efficiency. Headquartered in Germany, nanosystec supports their customers worldwide with subsidiaries in Asia and North America. The product portfolio includes high precision Active Alignment and Laser Welding Systems, Alignment and Epoxy Gluing Stations, Laser Soldering and Pick-and-Place Systems. New: Optical and electrical characterization and assembly for Silicon Photonics Devices. Working with quickly removable carriers reduces the expensive machine time to the core process of alignment and assembly. Loading and unloading takes only seconds. This concept also facilitates manufacturing different devices on the same station without change-over times from one process to the other. The versatile software package and a modular hardware concept allow for an infinite life time as the systems can be adapted to changing requirements over decades.

Booth: 51

Nikon Precision Inc.

1399 Shoreway Road
Belmont, CA 94002
(P) 512-943-4710
(E) brenden.wells@nikon.com
www.nikonprecision.com

Nikon Precision provides sales, marketing, and unparalleled support for Nikon Lithography systems worldwide. Our extensive product portfolio includes specialized solutions for MEMS/LED, packaging (backend), and flat panel display (FPD) processing, as well as advanced i-line, KrF, ArF, and immersion lithography systems used throughout the semiconductor and thin-film magnetic head (TFH) industries. Nikon MEMS Steppers provide extremely diverse processing capabilities. They are successful in meeting customers' unique requirements for not only HDD/LED and MEMS applications, but also for discretes, packaging (backend) applications, and more. Nikon continues to focus on expanding MEMS Stepper capabilities to meet varied performance and budgetary objectives for our customers. Newly developed systems maximize productivity, support substrates up to 200 mm and beyond, and enhance imaging with ghi/i-line capabilities. Nikon MEMS Steppers also provide a high degree of alignment flexibility, and the majority of MEMS Steppers support critical Backside Alignment (BSA) capabilities as well. In addition, a multitude of add-on functions further boost system performance and yield are available. Please visit our website at https://www.nikonprecision.com.

Booth: 21

NTK Technologies

3979 Freedom Circle Drive, Suite 320
Santa Clara, CA 95054
(P) 408-562-5124
(E) mstoops@ntktech.com
www.ntktech.com

NTK Technologies is a leader in IC Ceramic Packaging. With global service centers, NTK offers a wide range of packaging materials and package design services for Medical, Automotive, SiP/MCM, MEMS, Opto, RF, CMOS Image Sensors, Hi-Rel, Satellite, FCBGA, FCCSP, FPGA, CPU and MPU applications. Monolithic package designs for Medical and Mobile applications. Optimum package designs for 10G, 40G, and 100/400G. Large and small scale Ceramic STFs are manufactured for high-speed/high density probe-cards for semiconductor wafer test. Large and small scale ceramic substrates can be configured with narrow pitches and a wide range of pin count capabilities. NTK supports fast paced product cycle times with our advanced design and production flows featuring high precision processes for fast turn-around with the highest quality.

Booth: 53

NXQ

385 Woodview Ave.
Morgan Hill, CA 95037
(P) 408-776-5190
(E) dgeder@neutronixinc.com
www.neutronixinc.com

Neutronix-Quintel (NXQ) is a leading provider of high performance mask alignment systems since 1978. NXQ is comprised of a team of seasoned industry veterans with vast experience in photolithography, providing their customers with the most robust solutions which have been derived from many years of customer driven innovations. NXQ has well over 1000 systems installed around the world used for various technologies such as MEMS, Compound Semi, Biomedical, Microfluidics, HB LED, WLP, 3DIC / TSV, 2.5D Interposer and HCPV. Prominent high volume manufacturing companies utilize NXQ's equipment for end products such as transceiver chip sets for cell phones and other wireless devices, medical sensors, automobile sensors, LED Lighting, military and defence electronics, IR detectors, optical devices used for communications and discrete devices. The company's products are also used extensively throughout the world at universities and research institutes and are recognized as one of the most versatile and flexible mask aligners in the marketplace. NXQ works closely with customers to innovate and develop new features that differentiate their products from the competition. The company continues to gain market share with customers that require equipment suppliers who can meet their stringent needs for cost, performance and reliability. With the recently release of the 300mm platform, NXQ is well positioned to maintain double digit growth.

Booth: 56

PacTech USA Inc.

328 Martin Ave
Santa Clara, CA 95050
(P): 408-588-1925
(E): info.usa@pactech.com
www.pactech.com

PacTech Packaging Technologies GmbH, (group member of NAGASE & CO., Ltd.) is headquartered in Nauen, Germany, with wholly-owned subsidiaries: PacTech USA - Packaging Technologies Inc. in Silicon Valley, USA and PacTech ASIA Sdn. Bhd. in Penang, Malaysia. PacTech is comprised of two unique advanced packaging units: 1- EQUIPMENT MANUFACTURING: PacLine 300 A50: Automatic ENIG & ENEPIG plating tools. SB²-Jet: Laser solder jetting tool Ultra-SB²: Wafer level solder ball transfer system LAPLACE: Laser-assisted flip-chip bonders 2- SUBCONTRACT SERVICES: Flip Chip and Wafer Level Package Bumping Services including ENIG or ENEPIG for UBM (solder bumping) or OPM (wirebond) Other services include: AOI, X-Ray, Repassivation, RDL, Wafer Thinning, Backmetal, Laser Marking, Dicing and Tape & Reel.

Booth: 63

Palomar Technologies

2728 Loker Ave. West
Carlsbad, CA 92010
(P) 760-931-3600
(E) marcom@bonders.com
www.palomartechnologies.com
Twitter: @PalomarTech

Palomar Technologies is a leading supplier of automated microelectronic assembly machines and contract assembly services with specialization in precision die attach, wire bonding and vacuum reflow processes. High-precision assembly systems enable customers to increase yield and reduce costs in the manufacturing of optoelectronic, RF and power module packages.

Booth: 65

Plasma-Therm, LLC

10050 16th St. North
St. Petersburg, FL 33716
(P) 727-577-4999
(E) nancy.messineo@plasmatherm.com
www.plasmatherm.com

Plasma-Therm® is a leading provider of advanced plasma processing equipment. Plasma-Therm systems perform critical process steps in the fabrication of integrated circuits, micro-mechanical devices, solar power cells, lighting, and components of products from computers and home electronics to military systems and satellites. Specifically, Plasma-Therm systems employ innovative technology to etch and deposit thin films. The company's Mask Etcher® series for photomask production has exceeded technology roadmap milestones for more than 15 years. Plasma-Therm's Singulator® systems bring the precision and speed of plasma dicing to chip-packaging applications. Manufacturers, academic and governmental institutions depend on Plasma-Therm equipment, designed with "lab-to-fab" flexibility to meet the requirements of both R&D and volume production. Plasma-Therm's products have been adopted globally and have earned their reputation for value, reliability, and world-class support. Customers consistently rank Plasma-Therm among the top equipment suppliers, with multiple awards in the annual VLSIresearch Customer Satisfaction Survey, including being named "Ranked 1st" Etch and Clean Equipment Supplier five years in a row.

Booth: 32

Rudolph Technologies

16 Jonspin Road
Wilmington MA 01887
(P) 978-253-6200
(E) info@rudolphtech.com
www.rudolphtech.com

Rudolph Technologies, Inc. is a leader in the design, development, manufacture and support of defect inspection, lithography, process control metrology, and process control software used by semiconductor and advanced packaging device manufacturers worldwide. Rudolph delivers comprehensive solutions throughout the fab with its families of proprietary products that provide critical yield-enhancing information, enabling microelectronic device manufacturers to drive down costs and time to market of their devices. Headquartered in Wilmington, Massachusetts, Rudolph supports its customers with a worldwide sales and service organization. Additional information can be found on the Company's website at www.rudolphtech.com.

Booth: 50

SETNA

343 Meadow Fox Lane
Chester, NH 03036
(P): 603-548-7870
(E): mphillips@set-na.com
www.set-na.com

High-accuracy Bonding Experience, Equipment, and Materials

SETNA is a Manufacturing and Marketing, Sales and Service Organization centered on our experience and know-how in high-accuracy bonding and the equipment, materials, competencies surrounding it. SET Bonders have been the world-standard for applications in which micron precision post bond accuracy is required, for more than twenty years the FC150 Series has been the tool of choice. The Ontos7 is our atmospheric plasma system designed for and dedicated exclusively to the semiconductor manufacturing and packaging industry. Our patented (and patent pending) equipment and processes provide a unique advantage to our customers to enable low-cost, high yield, high-speed, chip-to-chip interconnect bonds at room temperature with minimal force.

Booth: 44

SHINKO

1280 East Arques Ave.
Sunnyvale, CA 94085
(P) 408-232-0499
(E) michael.hudgens@shinko.com
www.shinko.com

SHINKO Electric Industries Co., LTD., is a leading manufacturer of semiconductor and microelectronic packaging products including Organic Laminate Build-up Substrates, Etched and Stamped Lead Frames, Integrated Heat Spreaders, and IC and Module Assembly. We manufacture a full line of Organic Substrate structures including coreless options offering enhanced electrical performance and package miniaturization. SHINKO also provides subcontract IC assembly services with an emphasis on packaging solutions such as PoP, SiP as well as advanced technologies such as Molded Core Embedded Package (MCeP®) and Module assembly and test in support of a wide range of markets. Founded in Nagano, Japan in 1946, SHINKO's headquarters and primary production plants continue to reside in the greater area. In addition to our production facilities, we also provide the ultimate in service and solutions for our customers with Sales and Engineering support Worldwide. Come visit us at booth #44 to learn more about our latest product offerings for fine pitch interconnection, miniaturization and high density mounting for 3D assembly. www.shinko.com

Booth: 35

Sikama International Inc.

118 E. Gutierrez Street
Santa Barbara CA 93101
(P) 805-962-1000
(E) phil@sikama.com
www.sikama.com

Sikama International designs, manufactures, and markets solder reflow & curing systems, wafer flux coaters and wafer washers. Our ovens feature a patented conduction plus convection heating technology and are used for Wafer Bumping, LED Die Reflow, BGA Re-balling, High Density Package Reflow, Lid Attach, Fluxless Gold Tin Reflow, Lead Frame Reflow and Curing among many other applications.

Booth: 14

SMART Microsystems Ltd

141 Innovation Drive
Elyria, OH 44035
(P) 650-714-1570
(E) bcooper@meptec.org
www.smartmicrosystems.com

Located in Northern Ohio, SMART Microsystems' facility has over 15,000 sq. ft. of ISO 6 (class 1000) and ISO 5 (class 100) cleanrooms. This state of the art facility, furnished with flexible equipment capabilities for assembling a high mix of materials and products, creates a turn-key solution for microelectronic package assembly of MEMS and sensors. From prototyping through market entry, SMART can help you reduce the total cost of product development. Prototype development and manufacturing capabilities include dicing, die attach/flip chip, vacuum solder reflow, wire bonding, and encapsulation. Their environmental life testing identifies reliability issues early in your MEMS sensor product development. They build early proof-of-concept samples as well as feasibility studies to help you avoid challenges that appear early in process development. SMART Microsystem's engineering team's expertise in MEMS sensor products has solved many of these challenges.

Booth: 33

Sonoscan, Inc.

2149 E. Pratt Blvd.
Elk Grove Village, IL 60007
(P) 847-437-6400
(E) info@sonoscan.com
www.sonoscan.com

Founded in 1973 and headquartered in Chicago, IL, Sonoscan®, Inc. is a worldwide leader and innovator in Acoustic Micro Imaging (AMI) technology. Sonoscan manufactures and markets acoustic microscope instruments and accessories to nondestructively inspect and analyze products. Our C-SAM® scanning acoustic microscope provides unmatched accuracy and robustness setting the standard in AMI for the inspection of products for hidden internal defects such as poor bonding, delaminations between layers, cracks and voids. In addition, Sonoscan offers analytical services through regional testing laboratories in Asia, Europe and the U.S. and educational workshops for beginners to advanced on AMI technology.

Booth: 42

SPTS Technologies Ltd

Ringland way
Newport. NP18 2TA
(P) 1633474000
(E) Enquiries@orbotech.com
www.spts.com/
Twitter: @SPTS_Tech

SPTS Technologies, an Orbotech company, designs, manufactures, sells, and supports advanced etch, PVD, CVD and thermal wafer processing equipment and solutions for the global semiconductor and micro-device industries, with focus on the Advanced Packaging, MEMS, high speed RF device, power management and LED markets. With the acquisition of SPTS, Orbotech is now able to offer a broader range of process solutions for Advanced Packaging, which includes Orbotech's UV Laser Drilling, Laser Direct Imaging and Precision 3D Printing solutions. SPTS operates three manufacturing facilities in the UK and US, and operates across 19 countries in Europe, North America and Asia-Pacific. For additional product or company information, please visit: www.spts.com www.orbotech.com

Booth: 30

Sputtering Components

375 Alexander Drive WW
Owatonna, MN 55060
(P) 507-455-9140
(E) sales@sputteringcomponents.com
www.sputteringcomponents.com

Sputtering Components designs and manufactures equipment used for physical vapor deposition of thin films. SCI's PVD products include rotary sputtering magnetrons (end blocks and magnetics) and complete vacuum coater lid systems.

Booth: 23

STATS ChipPAC

46429 Landing Parkway
Fremont, CA 94538
(P) 510-979-8000
(E) contact.sales@statschippac.com
www.statschippac.com
Twitter: @STATSChipPACLtd

STATS ChipPAC is a leading service provider of semiconductor package design and characterization, wafer bump, assembly and test solutions for diverse end market applications in communications, digital consumer, computing and automotive electronics. STATS ChipPAC is a member of the JCET group of companies. JCET is one of the top semiconductor packaging and test providers in the world and the largest OSAT provider in China. Headquartered in Jiangyin, China, JCET has an extensive global manufacturing base with operations in China, Singapore and South Korea. The comprehensive packaging portfolio of JCET and its subsidiaries include discrete, leaded, laminate, flip chip, Molded Interconnect System, wafer level packaging and System-in-Package technologies. For more information, visit www.statschippac.com or www.jcetglobal.com.

Booth: 62

StratEdge Corporation

6335 Ferris Square Suite "C"
San Diego, CA 92121
(P): 858-569-5000
(E): c.stanley@stratedge.com
www.stratedge.com

StratEdge designs and manufactures electronic packages as well as provides assembly and test services. We have a complete line of post-fired and molded ceramic semiconductor packages operating from DC to 50+ GHz. Our patented electrical transition designs give StratEdge packages exceptionally low electrical losses, even at 50 GHz. Markets served include telecom, mixed signal, VSAT, broadband wireless, satellite, military, test and measurement, automotive, and MEMS. All packages are lead-free and most meet RoHS and WEEE standards. StratEdge is an ISO 9001:2008 facility. Please visit us at www.StratEdge.com or call 858-569-5000.

Booth: 31

Superior Silica

2450 W Broadway Rd, Ste 117
Mesa, AZ 85202
(P): 480-968-6637
(E): info@superiorsilica.com
www.superiorsilica.com

Superior Silica LLC is a chemistry-first company based out of Phoenix, AZ that specializes in manufacturing highly monodisperse silica nanoparticles and microspheres at industrial scales. Our proprietary process technology enables us to target a particular size better and more consistently than anyone in the world. We also manufacture particles with customizable surface chemistries to couple with specific polymeric matrices in device packaging applications. We are extremely cost-competitive and our manufacturing facility is located in Mesa, AZ. We look forward to meeting prospective customers at Device Packaging 2018 at Booth 31.

Booth: 25

Technic

300 Park East Drive
Woonsocket RI 02895
(P) 401-785-8763
(E) bsheeran@technic.com
www.technic.com/applications/semiconductor

Technic supplies some of the most advanced chemistry solutions for semiconductor packaging applications in the industry. High performance product development with application specific characteristics and unparalleled analytical expertise provides customers with the essential tools to meet the challenges of today's semiconductor manufacturing. Technic's semiconductor advanced packaging electrodeposition chemistries, marketed under the name Elevate, are well respected for innovation and high quality and are used in many applications including RDL, pillars, microbumps and LED packaging. In addition Technic supplies photoresist strippers for liquid and dryfilm resist as well as metal etchants for a variety of metals. Technic also offers analytical control systems. Technic's RTA (Real Time Analyzer) has become the leading analytical control system for damascene copper processes. The capability of the RTA system has now been successfully expanded into backend packaging applications for controlling TSV and copper pillar processes.

Technic Inc is a Rhode Island based privately held corporation with over 900 employees worldwide and currently operates over 20 global facilities in 14 countries within North America, Asia and Europe.

Booth: 20

TechSearch International, Inc.

4801 Spicewood Springs Rd., Ste. 150
Austin, TX 78759
(P) 512-372-8887
(E) tsi@techsearchinc.com
www.techsearchinc.com

TechSearch International, Inc. has a 28-year history of market and technology trend analysis focused on semiconductor packaging, materials, and assembly. Research topics include WLP, FO-WLP, Flip chip, CSPs including stacked die, BGAs, 3D ICs with TSVs, 2.5D interposers, and System-in-Package (SiP), embedded components, ADAS and automotive electronics and panel-based processing. In conjunction with SavanSys Solutions, wire bond, flip chip, WLP, and 3D IC cost models are offered. TechSearch International professionals have an extensive network of more than 18,000 contacts in North America, Asia, and Europe and travel extensively, visiting major electronics manufacturing operations and research facilities worldwide.

Booth: 57

Teikoku Taping System, Inc.

5090 North 40th Street, Suite 140
Phoenix, AZ 85018
(P): 480-794-1926
(E): joe.umpleby@teikoku-taping.com
www.teikoku-taping.com

For more than 25-years Teikoku Taping System has been an innovative leading custom equipment supplier for the backend semiconductor industry.

Teikoku's backend semiconductor products include Wafer Mounting Systems, UV Irradiation Systems, Tape Removal Systems, Backgrind Tape Laminators, and Dry Film Resist Laminators. TTS will continue to revolutionize the semiconductor industry and exceed industry expectations with new and innovative equipment designs.

Booth: 1

Unisem

2241 Calle de Luna
Santa Clara, CA 95054
(P) 408-734-3222
(E) info@unisemgroup.com
www.unisemgroup.com

Unisem is a global provider of semiconductor assembly and test services for many of the world's most successful electronics companies. Unisem offers an integrated suite of packaging and test services such as wafer bumping, wafer probing, wafer grinding, a wide range of leadframe and substrate IC packaging, wafer level CSP and RF, analog, digital and mixed-signal test services. Our turnkey services include design, assembly, test, failure analysis, and electrical and thermal characterization. With approximately 7,700 employees worldwide, Unisem has factory locations in Ipoh, Malaysia; Chengdu, People's Republic of China and Batam, Indonesia. The company is headquartered in Kuala Lumpur, Malaysia.

Booth: 60

UNITY SC

611 Rue Aristide Berges
38330 Montbonnot Saint Martin
(P) +33 4 56 52 68 00
(E) s.pottier@unity-sc.com
www.unity-sc.com

Unity SC (A FOGALE Nanotech Company) disclosed two new metrology solutions for advanced packaging applications. T-MAP 3D: Time-domain Optical Coherence is the most robust solution for TSV depth, bow & warp and individual layer TTV of a stack measurement as each interface is detected in the right order over a larger range than spectral interferometry. The only limitation is the minimum measurable thickness due to the high coherence length of the IR LED source. A new Near-Infrared Interferometer was recently developed at Fogale Nanotech Laboratories. The spectral bandwidth was increased to 110 nm, i.e. the minimum detectable optical thickness was improved by a factor of nearly three. This technology has been implemented into the Unity SC T-MAP series. NST 300: The NST 300 has been qualified by a major customer for CMP process control performed prior to 3D hybrid bonding process used in BSI (Back Side Imager) manufacturing. The tool is able to measure nanoscale topography at die level and at the extreme edge of the wafer with high lateral resolution and from several hundred of nm to few nm level of amplitude. Mechanical profilometry comparisons have shown good potential to perform measurement on wafers without metal layer coating. This represents a key advantage for inline control, as the technology will allow higher throughput than mechanical profilometry and the ability to give much more information to tune and control the CMP process.

Booth: 61

XYZTEC, Inc

55 Sterling Street
Clinton, MA 01510
(P) 978-880-2598
(E) tom.haley@xyztec.com
http://www.xyztec.com

XYZTEC manufactures bond testers that satisfy military, medical and semiconductor process engineering requirements. Our award winning Rotating Measurement Unit allows users to switch from one test to another within a few seconds. The entire bond test process can be fully automated such that operators no longer have to sit in front of a machine all day to perform wire pull or shear testing. See us at Booth 61.

Booth: 64

Yield Engineering Systems, Inc.

203A Lawrence Drive
Livermore, CA 94551
(P) 925-373-8353
(E) info@yieldengineering.com
www.yieldengineering.com

Yield Engineering Systems (YES) provides a wide variety of processing equipment including high reliability dielectric vacuum cure ovens for Fan-Out Wafer Level Packaging (FOWLP) and Redistribution Layers (RDL) type processes. YES tools offer fast polymer cure cycle, excellent thermal, electrical and mechanical properties, reliable multi-level interconnections and proper cross-linking. YES Applications Manager, Ken Sautter, will be leading a technical session on Tuesday, March 6, 2018 at 5:00 PM titled "Addressing the Challenges of Multi-layer Polymer Processing for Fan-Out Wafer Level Packaging". YES will also be participating in the Interactive Poster Session on Wednesday, March 7, 2018 at 5:30 PM discussing the topic. Our tool line features dielectric vacuum cure ovens, silane vapor phase deposition systems, high vacuum ovens, plasma clean ovens, HMDS prime/image reversal ovens and plasma strip/descum systems. YES photoresist/ descum systems provide excellent strip rates for photoresist, polyimide and organics removal processes. Quality process equipment, built for process engineers.

Booth: 36

Yole Developpement

75 cours Emile Zola
Villeurbanne, 69006 France
(P): 33-472-83-01-80
(E): fabre@yole.fr
www.yole.fr

Meet with Yole Développement analysts at booth #36 and discuss with them the latest advanced packaging dynamic market trends!

Booth: 54

Yxlon FeinFocus

5675 Hudson Industrial Parkway
Hudson, OH 44236
(P) 480-432-0840
(E) randy.floyd@yxlon.com
www.yxlon.com

YXLON is a leading supplier of industrial X-Ray inspection and CT solutions for the non-destructive testing of materials and electronics. The YXLON product portfolio includes the FF20, FF35, and the new Cheetah EVO and Cougar EVO series which offer effortless high-quality X-Ray imaging for a wide range of continuous inspection tasks. The Cheetah EVO and Cougar EVO combine proprietary FeinFocus technology with advanced high-speed flat panel detector technology. The FF20 and FF35 provide highest resolution and precision CT results. Within seconds, the systems adapt between inspection tasks-failure analysis, research and development, process control and product testing including QuickScan mode.

Booth: 27

Zuken, Inc.

1900 McCarthy Blvd. Suite 400
Milpitas, CA 95035
(P) 408-890-2831
(E) Humair.Mandavia@zukenusa.com
www.zukenusa.com

Zuken is a global provider of leading-edge software and consulting services for system-level electrical and electronic design and manufacturing. Founded in 1976, Zuken has the longest track record of technological innovation and financial stability in the electronic design automation (EDA) software industry for advanced packaging, printed circuit board design, and multi-domain co-design. The company's extensive experience, technological expertise and agility, combine to create world-class software solutions. Zuken's transparent working practices and integrity in all aspects of business produce long-lasting and successful customer partnerships that make Zuken a reliable long-term business partner. Zuken is focused on being a long-term innovation and growth partner. The security of choosing Zuken is further reinforced by the company's people—the foundation of Zuken's success. Coming from a wide range of industry sectors, specializing in many different disciplines and advanced technologies, Zuken's people relate to and understand each company's unique requirements.

Don't Miss the Technical Session on Tuesday, March 6th @ 5 PM :

Addressing the Challenges of Multi-layer Polymer Processing for **Fan-Out Wafer Level Packaging**

Ken Sautter, Applications Manager

Visit YES @ Booth #64

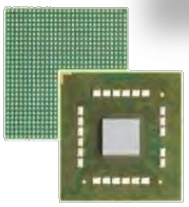
featuring

Dielectric Vacuum Cure Ovens *for* **FOWLP/RDL Application Solutions**

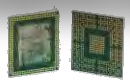
KYOCERA

Electronic Packaging, Devices, and Assembly for Medical, Biotech, and IoT Applications

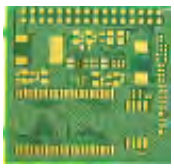
Organic Packages



Flip-Chip Ball-Grid Array (FCBGA)



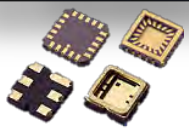
Flip-Chip Chip-Scale Package (FCCSP)



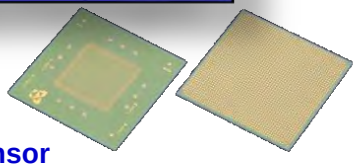
Components-Embedded Module Substrate

New! Blood Flow Sensor Device

Ceramic Packages

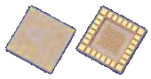


MEMS / Sensor Package



HITCE Package

Packages for Wireless Communication



LTCC-Cu, Au, Ag Antenna pkg w/ Platinum

Package Assembly

- Flip Chip
- Wire Bond
- SMD
- BGA Ball Attachment
- Lid Attach
- Vacuum Solder / Die Attach
- Precision Pick & Place
- Low to mid-volume
- Prototype and engineering with quick-turn
- Class 100 - 1000 Clean Rooms

Integrated Flip Chip & Wire Bond Assembly

Kyocera International, Inc. 8611 Balboa Ave. San Diego, CA 92123

Phone: (800) 468-2957

ISO 9001 / 14001

E-mail: kaicorp@kyocera.com

Website: http://americas.kyocera.com/kai/semiparts

10-27-2017

MONDAY, MARCH 5, 2018	Pre-Conference: PDCs & Welcome Reception
7:00 am – 7:00 pm	*REGISTRATION*
10:00 am – 5:30 pm	*PROFESSIONAL DEVELOPMENT COURSES (PDCs)*
5:30 pm – 7:30 pm	WELCOME RECEPTION (All Attendees Are Invited To Attend)

Thank You to the Premier Sponsors:

ASE GROUP

EMD Performance Materials

XYZTEC

Amkor Technology

NAMICS

cadence

Mentor Graphics

KYOCERA

TUESDAY, MARCH 6, 2018 — Morning Technical Sessions

7:00 am – 7:00 pm	*REGISTRATION OPEN*
7:00 am – 8:00 am	*BREAKFAST SPONSORED BY:* EMD Performance Materials · XYZTEC
8:00 am – 8:20 am *ROOM 107-108*	*OPENING COMMENTS* *General Chair: Peter Ramm, Fraunhofer EMFT Munich* *KEYNOTE SESSIONS SPONSORED BY:* SPTS (An orbotech Company)
8:20 am – 9:05 am *ROOM 107-108*	KEYNOTE 1 **3D-IC: Past, Present and Future** *Though the process flows and technologies required to implement 3DIC were being developed in the late 1980's and early 1990's by pioneers such as Mitsu Koyanagi in Japan and Peter Ramm in Germany, the decade of 3DIC started in earnest in the 2007-2008 timeframe with the commercial announcement by Toshiba of CMOS Image sensor modules with TSV. This was quickly followed by announcements from Samsung, IBM and TSMC indicating that 3DIC was the key technology to future integration and would in some ways be the savior to our industry as scaling, as described by "Moore's Law" slowly came to an end. In this presentation we will take a look at how 3DIC has developed over the decade, where we are and where we are going.*  ***Phil Garrou, Microelectronic Consultants of NC*** *Dr. Philip Garrou retired from Dow Chemical in 2004 as Global Director of Technology for their Advanced Electronic Materials business unit. He is now contributing editor and blogger ("Insights from the Leading Edge") for Solid State Technology, a subject matter expert (SME) for DARPA and runs his consulting company Microelectronic Consultants of NC in the RTP area.*
9:10 am – 9:55 am *ROOM 107-108*	KEYNOTE 2 **2D to 3D Package Architectures - Back to the Future** *Moore's Law Scaling has driven electronics industry growth and new package architectures (including 3D architectures and architectures currently defined as 2.1D, 2.3D or 2.5D architectures) are projected to be major enablers to maintain the pace of Moore's law scaling and enable heterogeneous integration. Historically, packaging has scaled sufficiently to act as a space and electrical transformer to enable transistor/silicon scaling, and innovations in packaging were focused on minimizing impact to the power, performance and latency of silicon. With an increasing drive for heterogeneous integration, packaging is being increasingly challenged to deliver power-efficient, high bandwidth on/off package low power links and meet diverse functionality ranging from high performance servers to flexible, wearable electronics. This talk will introduce a new IEEE standardized industry nomenclature on package architectures covering and clearly demarcating both 2D and 3D constructions, as well as highlight the key metrics driving the evolution of these architectures, their current values (based on the state of the art) and projections for the next 5-10 years. This is expected to drive focus and direction to industry, academia and government on critical technology trends and motivations for research needed to meet next generation requirements in the 2D-3D architecture space.*  ***Dr. Raja Swaminathan, Package Architect, Intel Corporation*** *Dr. Raja Swaminathan is an IEEE senior member and is a package architect at Intel for next generation server, client and mobile products. His expertise is on delivering integrated HVM friendly package architectures with optimized electrical, mechanical, thermal solutions. He is an IEEE, ITRS and iNEMI roadmap author on packaging and design. He has also served on IEEE micro-electronics and magnetics technical committees. He has 26 patents and 25 peer-reviewed publications and holds a Ph.D. in Materials Science and Engineering from Carnegie Mellon University.*
10:00 am – 6:30 pm	*EXHIBITION AND TECHNOLOGY SHOWCASE*
10:00 am – 10:30 am	*BREAK IN THE EXHIBIT HALL SPONSORED BY:* INTEVAC

Be sure to visit our exhibitors to see the latest technologies & services:

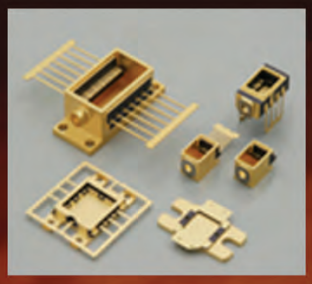
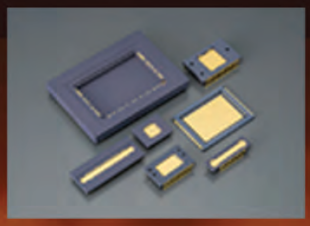
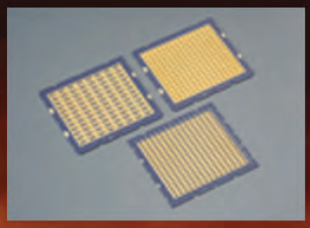
Tuesday, March 6, 2018 - 10:00 AM - 6:30 PM | Lunch, Breaks and a Reception will be held in the Exhibit Hall

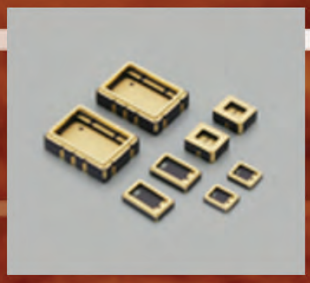
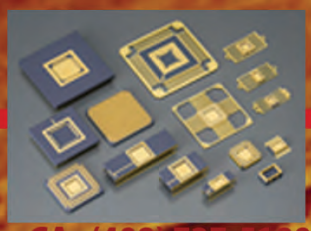
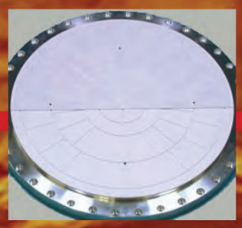
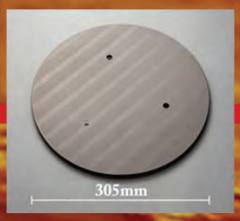
Wednesday, March 7, 2018 - 10:00 AM - 4:00 PM | Lunch, and Breaks will be held in the Exhibit Hall

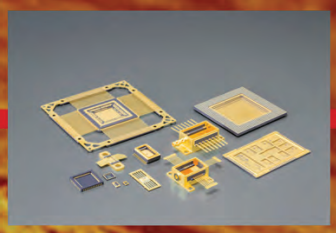
Forging Innovation and Partnerships

Advanced Technical Ceramics

Packaging for every application



Clara, CA (408) 727-5180

IGNITE YOUR SPIRIT

NGK SPARK PLUGS | NTK TECHNICAL CERAMICS

NTK TECHNOLOGIES, INC.

www.ntktech.com US Headquarters: 3979 Freedom Circle, Santa Clara, CA 408) 727-5180
scdinfo@ntktech.com

	Interposers, 3D IC & Packaging *ROOM 104-106*	Fan-Out, Wafer Level Packaging & Flip Chip *ROOM 107-108*	Engineered Micro Systems/Devices *(including MEMS & Sensors)* *ROOM 102-103*
TUESDAY MORNING SESSIONS	TA2: APPLICATION - SiP Chairs: Rama Puligadda, Brewer Science; Diane Scheele, Versum Materials	TA2: FAN-OUT WAFER LEVEL PACKAGING; TECHNOLOGY Chairs: John Hunt, ASE Group; Rebecca Schmidt, DOW Electronic Materials	TA3: RF & QUANTUM DEVICES Chairs: Li-Anne Liew, UC Boulder / NIST; and Keaton Rhea, Auburn University
10:30 am – 11:00 am	081 Market and Technology Trends of Advanced Packaging for SiP Application Santosh Kumar, Yole Developpement	006 Cost and Yield Analysis of RDL Creation in Fan-out Wafer Level Packaging Amy Lujan, SavanSys Solutions LLC	005 A Wafer-Bonding Method for Fabricating Integrated GaAs Schottky Varactor Multipliers on Silicon Platforms Robert M. Weikle II, University of Virginia (Linli Xie, Souheil Nadri, Naser Alijabbari, Masoud Jafari, Michael E. Cyberey, N. Scott Barker, Arthur W. Lichtenberger)
11:00 am – 11:30 am	077 Multi-die Connectivity and the Proposition for Heterogeneous IC Packaging Mike Kelly, Amkor Technology	020 Embedded Wafer Level Ball Grid Array as One Solution for 2.5D System in Package Jacinta Aman Lim (STATS ChipPAC)	022 Quasi-Optical Directional Coupler for Ultra-Wideband THz Vector Network Analyzers Yiran Cui, Arizona State University (Georgios C. Trichopoulos)
11:30 am – 12:00 pm	014 Improving Solder Joint Reliability in SiPs Using Plasma-Based Nanocoating for Top Coat Simon McElrea, Semblant	028 Moving from Wafer Level Packaging to Panel Format Henning Hübner, Atotech Deutschland GmbH (Christian Ohde, Ralph Zoberbier, James Welsh)	054 Nonequilibrium Transport in the Pseudospin-1 Dirac-Weyl System Cheng-Zhen Wang, Arizona State University (Hong-Ya Xu, Liang Huang, and Ying-Cheng Lai)
12:00 pm – 12:30 pm	064 3D Modular Power Electronic Systems, based on Embedded Components Lars Boettcher, Fraunhofer IZM Berlin (S. Karaszkiewicz , Th. Löher, D. Manessis , and A. Ostmann)	066 Innovative Wafer Fan-out Technologies -- Heterogeneous Integration for a Connected World Curtis Zwenger, Amkor Technology (WonChul Do, Eoin O'Toole)	050 Out-of-Time-order Correlator in billiard systems Chendi Han, Arizona State University (Hongya Xu, Ying-Cheng Lai)
12:30 pm – 2:00 pm	*LUNCH IN THE EXHIBIT HALL SPONSORED BY:* (Food served from 12:30 pm - 1:30 pm) ASE GROUP		

	Interposers, 3D IC & Packaging *ROOM 104-106*	Fan-Out, Wafer Level Packaging & Flip Chip *ROOM 107-108*	Engineered Micro Systems/Devices *(including MEMS & Sensors)* *ROOM 102-103*
TUESDAY AFTERNOON SESSIONS	TP1: TSV / TGV / 3DIC Chairs: Lars Böttcher, Fraunhofer IZM; Stevan Hunter, ON Semiconductor	TP2: FAN-OUT WAFER LEVEL PACKAGING; APPLICATIONS Chairs: Amy Lujan, SavanSys Solutions; Curtis Zwenger, Amkor Technology	TP3: CHAOTIC & NONLINEAR SYSTEMS Chairs: Ned Corron, US Army AMRDEC; Aubrey Beal, US Army AMRDEC
2:00 pm – 2:30 pm	029 2018 A TURNING POINT FOR 3D TSV INTEGRATION: WILL AI BE THE REAL OPPORTUNITY FOR 3D AND 2.5D INTEGRATION? Emilie Jolivet, Yole Developpement (Thibault Buisson)	009 Fan-Out Wafer-Level-Packaging: Market and Technology Trends Jerome Azemar, Yole Developpement	002 Large Class of Optimal Communication Waveforms Exhibit Chaos Marko Milosavljevic, U. S. Army Aviation & Missile Res., Dev., & Eng. Center (Ned Corron, Jonathan Blakely)
2:30 pm – 3:00 pm	026 3d Die Stacks w/o TSVs that Operate at Comparable High Bandwidth and Power Efficiency Dev Gupta, APSTL llc	067 Packaging and Integration Strategy for mmWave Products Urmi Ray, STATS ChipPAC, Inc.	042 Wireless Communication Demonstration in Hardware Using an Exactly Solvable Chaotic System D. Aaron Whitney, Auburn University (Benjamin K. Rhea, Andrew Muscha, Frank Werner, R. Chase Harrison, Robert Dean)
3:00 pm – 3:30 pm	073 Advantages of through glass via (TGV) for RF Front End Pramodh Bangaloremadhuranath, Corning Incorporated	044 Packaging and Assembly Challenges for Automotive ADAS Linda Bal, TechSearch International, Inc (E. Jan Vardaman)	036 Chaos in a Linear Wave Equation Ned Corron, US Army AMRDEC
3:30 pm – 4:00 pm	*BREAK IN THE EXHIBIT HALL SPONSORED BY:* TechSearch INTERNATIONAL		
4:00 pm – 4:30 pm	035 Rapid Physical Prototyping of Microelectronic Systems using Heterogeneous Technologies with Silicon Interposers Gord Harling, Innotime Technologies (Frederick Kalinian)	069 Panel Chip Last Fan-out Warpage Analysis and Control Strategy Ian Hu, ASE (Pohsien Sung, Meng-Kai Shih, David Tarng, CP Hung, JY On, Dinos Huang)	037 Szilard's Information Engine: Recent Progress and a Chaotic Analog Aubrey Nathan Beal, U.S. Army AMRDEC (Jonathan N. Blakely)
4:30 pm – 5:00 pm	043 Glass Solutions for Packaging and RF MEMs Aric Shorey, Corning Incorporated (Jay Zhang)	052 Comparison of electrical performance between FO WLP and Flip Chip on Coreless Substrate (FC - CLS) packages Dev Gupta, APSTL	017 Non-autonomous Chaotic Circuit that Integrates a Variable Forcing Function on to a Single PCB Benjamin K. Rhea, Auburn University (R. Chase Harrison, Robert Dean)
5:00 pm – 5:30 pm	046 Progress in Time-Domain Optical Coherence Tomography for TSV/3Di stacking Metrology Dario Alliata, UnitySC (Guillaume Vienne, UnitySC; Charankumar Godavarthi, Eric Legros, Jean-Philippe Piel, Philippe Parbaud, Christian Néel, Fogale Nanotech)	071 Addressing the Challenges of Multi-layer Polymer Processing for Fan-Out Wafer Level Packaging Ken Sautter, Yield Engineering Systems, Inc.	051 Stretching Time in FPGAs: Chaos Enhanced Entropy using Asynchronous Logic Seth Cohen, Southern Research (Ned Corron, US Army AMRDEC)
5:30 pm – 6:30 pm	*EXHIBIT HALL RECEPTION SPONSORED BY:* NGK SPARK PLUGS | NTK TECHNICAL CERAMICS NTK TECHNOLOGIES, INC. DOW TECHNIC		
6:30 pm – 8:00 pm	**EVENING PANEL DISCUSSION:** *Advanced Packaging – What's New? What's Missing? What's Next?* *Details on the following page…*		

JOIN US FOR DEVICE PACKAGING 2018

March 4-7, 2019 | WeKoPa Resort | Look for Details at Registration! Contact bschieman@imaps.org to participate.

6:30 pm – 8:00 pm	**EVENING PANEL DISCUSSION** *Advanced Packaging – What's New? What's Missing? What's Next?* *Driven by a continuously increasing number of new applications for instance in the field of IoT with integrated sensor and MEMS; different types of 5G connectivity solutions and mobile communication infrastructure; Automotive electronics for engine and transmission, chassis, safety, driver assistance, passenger comfort and infotainment; faster datacenters with more memory for big data; more space for battery and display in next generation mobile phones; next generation imaging and image recognition systems in mobile devices; power electronics; processing cryptocurrency; … advanced packaging as indispensable part of the final product is facing new challenges in achieving required higher performance, smaller form-factor, higher reliability levels and lower cost. Can existing packaging technologies be extended to meet those requirements? Will large format Panel-Level Packaging bring a cost down? Are new packaging technologies needed? Who will drive and pay the development of those? Will more packaging and test be done by IDMs and Foundries in future instead by OSATs? What is done to get Wafer-Level Chip-Scale Packaging, Fan-Out Wafer-Level Packaging, Heterogenous Integration, System-in-Package and 3D Packaging ready to answer those new challenges? The industry experts in this evening panel discussion will present their view on this and intensively discuss with the audience. Be sure to bring your burning questions about Advanced Packaging – What's new? What's missing? What's next?* *Moderator:* *Urmi Ray, Senior Director, Group Technology Strategy, StatsChipPac* *Panelists:* *Glenn Daves, Head of Package Innovation, NXP Semiconductors N. V.* *Erica Folk, Manager, MMIC/RFIC Design, Northrop Grumman* *Ravi Mahajan, Fellow, Co-Director High Density Interconnect Pathfinding, Intel* *Paul Mescher, Principal Packaging Technologist, Microsoft* *Susan Trulli, Sr. Engineering Fellow, Raytheon Company* ***Panel Session & Refreshments Sponsored by:*** YES Yield Engineering Systems, Inc.

WEDNESDAY, MARCH 7, 2018 — GBC Keynote & Plenary Session

7:00 am – 7:00 pm	*REGISTRATION OPEN*
7:00 am – 8:00 am	*BREAKFAST SPONSORED BY:* EMD Performance Materials · XYZTEC

iMAPS Global Business Council

Welcome to the Global Business Council (GBC) Keynote & Plenary Session on

AUTOMOTIVE SYSTEMS DRIVING NEW MICROELECTRONICS OPPORTUNITIES

8:00 am – 8:15 am	OPENING COMMENTS: GBC Chairs: Lee Smith, (UTAC) United Test & Assembly Center; Thomas Goodman, Izinus
8:15 am – 9:00 am	GBC KEYNOTE: ***PACKAGING AND THE AUTONOMOUS CAR*** *Autonomously driving cars are the near goal for many ongoing development efforts in the automotive industry. Electronics systems required to accomplish this end continue to evolve. Even so, system architectural and component decisions are becoming clear, including sensing requirements, workload partitioning between centralized and distributed computing nodes, security, and communications. These combine to drive great diversity in the types and capabilities of the microelectronic packaging required to support them. The interplay between self-driving system components and architecture on the one hand and, on the other, the packaging required will be expanded and explored, with relevant examples given.*  ***Glenn G. Daves, Head of Package Innovation, NXP Semiconductors N. V.*** *Glenn G. Daves is Vice President of Package Innovation at NXP Semiconductors. He is responsible for package design, technology development, and assembly process development in support of NXP's full product portfolio. NXP serves diverse markets, each diving unique requirements: automotive (where NXP is the #1 supplier in the industry), handheld, consumer, industrial, banking, medical, and military. Prior joining NXP, Glenn led packaging and printed circuit board development for Freescale Semiconductor. Prior to that, he led global packaging product and technology development at the IBM Corporation. He has also held leadership positions in project management, test and burn-in engineering, and assembly manufacturing engineering. Glenn holds twenty-seven U.S. patents and has degrees from Brown University, the University of Illinois at Urbana-Champaign, and Alliance Theological Seminary.*
9:00 am – 9:30 am	Market Drivers and Packages for Automotive Electronics: What's New and What's Not? Jan Vardaman, TechSearch International
9:30 am – 10:00 am	MEMS & Sensors for Next Generation Automotive Santosh Kumar, YOLE
10:00 am – 4:00 pm	*EXHIBITION AND TECHNOLOGY SHOWCASE*
10:00 am – 10:45 am	*BREAK IN THE EXHIBIT HALL SPONSORED BY:* INTEVAC
10:45 am – 11:15 am	Automotive Packaging: Evolution, Development and Integration Shaun Bowers, Amkor Technology, Inc.
11:15 am – 11:45 am	Package Integration at Chip and System Level for Automotive Electronics Venky Sundaram, Georgia Tech
11:45 am – 12:00 pm	GBC CLOSING REMARKS: GBC Chairs: Lee Smith, (UTAC) United Test & Assembly Center; Thomas Goodman, Izinus
12:00 pm – 1:30 pm	*LUNCH IN THE EXHIBIT HALL SPONSORED BY:* *(Food served from 12:00 pm - 1:00 pm)* ASE GROUP

	Interposers, 3D IC & Packaging *ROOM 104-106*	Fan-Out, Wafer Level Packaging & Flip Chip *ROOM 107-108*	Engineered Micro Systems/Devices *(including MEMS & Sensors)* *ROOM 102-103*
WEDNESDAY AFTERNOON SESSIONS	WP1: 3D ARCHITECTURES AND PROCESSES Chair: Rahul Jain, Intel; Gilles Poupon	WP2: FAN-OUT WAFER LEVEL PACKAGE ASSEMBLY; EQUIPMENT AND MATERIALS Chairs: Steffen Kroehnert, Amkor Technology; Anup Pancholi, Intel Corp.	WP3: MEMS & SENSORS Chairs: Robert Weikle, University of Virginia; Robert Dean, Auburn University
1:30 pm – 2:00 pm	076 3D and Advanced Packaging Trends in Foundry Space Hamid Eslampour, GlobalFoundries	004 Direct Metal Replenishment - Cost-effective Novel Method of Replenishing Electrolytic Plating Baths I. Popova, Ancosys GMBH (H. Cox, C. Rueckl, A. Zhang, J. Stahl)	048 **Micro Acoustic Metamaterial for Sound Attenuation** Fuxi Zhang, Auburn University (George Flowers, Robert Dean)
2:00 pm – 2:30 pm	074 Wafer Nano Topography and Edge Roll-Off Metrology for 3D Monolithic Integration Dario Alliata, UnitySC (Carlos Beitia, M. Abdel Sater, L. Brunet, N. Devanciard, V. Balan, C. Euvrard, Y. Exvrayart, C. Laborderie, CEA LETI; S. Godny, J-F. Boulanger, S. Petitgrand, Y. Guillou, G. Fresquet, UnitySC)	011 Underfill Dispensing for Chip-on-wafer Akira Morita, Nordson Asymtek (WeiWei Gu, Brian Chung)	049 **Environmentally Isolating Packaging for MEMS Sensors** Michael Kranz, EngeniusMicro (Michael Whitley, Carl Rudd, EngeniusMicro, Jeff Craven II, Steven Clark, Robert Dean, George Flowers, Mark Adams, Auburn University)
2:30 pm – 3:00 pm	080 Achieving Monolithic SoC Performance with a Lower Cost, Rapidly Upgradeable 2.5D Modular Architecture: Challenges and Opportunities Pavel Borodulin, Northrop Grumman	033 Flux Apply, Reflow and Clean in a Single Integrated Tool Gary Hillman, S-Cubed (Daniel Leske AEMTech, Berlin)	057 Low Pressure Ratio Cascaded Joule-Thomson Cryogenic Coolers Collin Coolidge, University of Colorado (Li-Anne Liew, Ray Radebaugh, Y.C. Lee)
3:00 pm – 4:00 pm	*BREAK IN THE EXHIBIT HALL SPONSORED BY:* SIP A New York State Center of Excellence BINGHAMTON UNIVERSITY		
4:00 pm – 4:30 pm	070 12:1 Aspect Ratio Mid-process TSV Integration and Functional Test Using Advanced Metallization Processes Christophe Aumont, STMicroelectronics (Gilles Romero, STMicroelectronics; Thierry Mourier, Mathilde Gottardi, Céline Ribière, Stéphane Minoret, Pierre-Emile Philip, CEA-LETI; Gaelle Guittet, Vincent Mevellec, Aveni)	040 Photo Sensitive PI/PBO for Low Temperature Cure Daisaku Matsukawa, Hitachi Chemical DuPont MicroSystems, Ltd. (Nobuyuki Saito, Satoshi Abe, Atsutaro Yoshizawa, Noriyuki Yamazaki, Tetsuya Enomoto, Takeharu Motobe, Yuhei Okada, Toshihisa Nonaka)	061 Design of Electrostatic Force Assisted, Piezoelectrically Driven Silicon Chip-based Compressor for Micro Vapor Compression Refrigeration Cooling Li-Anne Liew, University of Colorado at Boulder, and National Institute of Standards and Technology (Ching-Yi Lin, Collin Coolidge, Y.C. Lee)
4:30 pm – 5:00 pm	023 Laser Full Cut Dicing of Thin Si IC wafers Jeroen van Borkulo, ASM Pacific Technologies (Paul Verburg, Richard van der Stam)	015 Linear Transport Degas, Pre-Clean, and PVD Processes for RDL Barrier/Seed Formation in Fan-Out Packaging Paul Werbaneth, Intevac, Inc. (Babak Adibi, Terry Bluck, Chun-Chung Chen, Daniel Gallagher, Vladimir Kudriavstev, Lisa Mandrell, Billy Runstadler, Chris Smith, Jim Sullivan)	047 A PCB Sensor for Improving Loggerhead Sea Turtle Nesting Research Rebecca Dean, Auburn University (Robert Dean)
5:00 pm – 5:30 pm		068 Canon Manufacturing Solutions for Advanced Heterogeneous Integration and Fan-Out Wafer Level and Panel Level Packaging Processes Doug Shelton, Canon USA (Tomii Kume, Sanjay Shinde, Takaaki Tsunoda)	060 3D TSV Inductors for Secure IoT Bruce Kim, City University of New York (Sang Bock Cho)

Post-Conference Presentations DOWNLOAD:

In Production Now – Available 1-2 Weeks After Conference

All full conference attendees & exhibitors will be emailed a link to download all of the technical presentation and exhibitor presentations from Device 2018

Speakers – slides left on the session laptops will be used. Or you MUST send updated file to bschieman@imaps.org *before the end of the conference*.

The DPC 2018 presentations will be ARCHIVED into IMAPS online research portal/library, IMAPSource®, around April 1st.

iMAPSource
Microelectronics Research Portal

www.imapsource.org

IMAPSource® currently features all of IMAPS proceedings, journal papers, magazines, and DPC/other conference publications back to 2010. This new portal is a fully searchable, ***Google Scholar***-friendly database.

Get Searching for DPC files today!

INTERACTIVE POSTER SESSION & HAPPY HOUR

Outside on Patio Overlooking Desert: 5:30 pm - 6:30 pm

(Poster Presenter Setup - 4:00 pm - 5:25 pm)

Poster Session & Happy Hour Sponsored by:

007
Sputtered Package Encapsulation Process Improvements with the use of Swing Cathode Rotary Magnetrons
Sarah Williams, Sputtering Components, Inc. (Patrick Morse)

008
The Impact of Glass Style and Orientation on the Reliability of SMT Components
Greg Caswell, DfR Solutions (Maxim Serebrini)

012
Effective Method for Wire Bonds Rework using Conductive Epoxy
Catherine Marsan-Loyer, MiQro Innovation Collaboration Center (C2MI) (Thomas Dequivre)

021
Mechanical Properties of Aluminum Bond Pad Structures with Different Thicknesses
Subramani Manoharan, University of Maryland (Carlos Morillo, Stevan Hunter, Patrick McCluskey)

024
The Application of Immersion Tin for QFN Production
Rick Nichols, Atotech Deutschland GmbH (Hubertus Mertens, Sandra Heinemann, Gustavo Ramos)

031
A Novel Temporary Adhesive for Solder Ball Attachment in Fluxless Reflow System
Hsiang Chuan Chen, Shenmao Technology Inc (Ruei-Ying Sheng, Chen-Yi Chen, Chang-Meng Wang)

045
Inkjet Printing Enables New Semiconductor Packaging Technologies
Wouter Brok, Meyer Burger BV (Erik Corduwener)

053
Fast In Situ Thermo Compression Flip Chip Bonding Process Optimized for 3D Die Stacking
Dev Gupta, APSTL llc

058
High-Temperature Thermal Interface Materials for Wide-bandgap (WBG) Applications
Sayangdev Naha, ADA Technologies (Mike Tomlinson, Daniel Cooney)

072
Temporary Bonding and the Challenge of Cleaning Post Debond
Phillip Tyler, Veeco PSP (Laura Mauer)

078
Integration of a Chemically-Amplified Photoresist and an Advanced Packaging Stepper for Advanced Packaging Technologies
Jack Mach, Rudolph Technologies (Keith Best, Roger McCleary, Rudolph Technologies; Rosemary Bell, Joseph Lachowski, Mitsuru Haga, Inho Lee, Regina Cho, Dow Electronic Materials)

****

071 -- *also in Session TP2*
Addressing the Challenges of Multi-layer Polymer Processing for Fan-Out Wafer Level Packaging
Ken Sautter, Yield Engineering Systems, Inc.

056 -- *also in Session THA3*
Successful FPGA Obsolescence Form, Fit, and Function Solution Using a MCM and DER™ to Implement Original Logic Design
Erick Spory, Global Circuit Innovations, Inc.

073 -- *also in Session TP1*
Advantages of through glass via (TGV) for RF Front End
Pramodh Bangaloremadhuranath, Corning Incorporated

004 -- *also in Session WP2*
Direct Metal Replenishment - Cost-effective Novel Method of Replenishing Electrolytic Plating Baths
I. Popova, Ancosys GMBH (H. Cox, C. Rueckl, A. Zhang, J. Stahl)

006 -- *also in Session TA2*
Cost and Yield Analysis of RDL Creation in Fan-out Wafer Level Packaging
Amy Lujan, SavanSys Solutions LLC

(additional abstracts might also be presented)

2018 3D InCites Awards Ceremony – *Immediately following the Poster Session (Hosted by IMAPS)*

Platinum Sponsors

THURSDAY, MARCH 8, 2018 — Morning Technical Sessions

7:00 am – 11:30 am	*REGISTRATION OPEN*
7:00 am – 8:00 am	*BREAKFAST SPONSORED BY:* EMD Performance Materials · XYZTEC
8:00 am – 8:45 am *ROOM 107-108*	*KEYNOTE SESSIONS SPONSORED BY:* SPTS (An orbotech Company) KEYNOTE 3 **The Growth of Heterogeneous Integration and the Importance of Electronic Materials**  ***Rozalia Beica, Global Director New Business Development, DOW Electronic Materials*** *Rozalia Beica is Global New Business Development Director at Dow Electronic Materials, focusing on identifying and developing new technology and business opportunities for advanced packaging and interconnects. Rozalia has 25 years of international working experience across various industries, including industrial, electronics and semiconductors. For 18 years she was involved in the research, applications and strategic marketing of Advanced Packaging and 3D interconnect technologies, with global leading responsibilities at specialty chemicals (Rohm and Haas), equipment (Semitool, Applied Materials and Lam Research) and device manufacturing (Maxim IC). Prior to joining Dow, Rozalia was the CTO of Yole Développement where she led the market research, technology and strategy consulting activities for Advanced Packaging and Semiconductor Manufacturing. Rozalia has a M.Sc in Chemical Engineering from Polytechnic University "Traian Vuia" in Romania, a M.Sc. In Management of Technology from KW University in the U.S. and an Global Executive MBA from Instituto de Empresa Business School in Spain.*
8:45 am – 9:30 am *ROOM 107-108*	KEYNOTE 4 **System Design Transition from PCB to SiP Solutions** *Smartphone, Internet of Things (IoT) and other consumer products demand extreme miniaturization, cost reduction, and continuous performance enhancements. Also, computing and networking products continuously need power reduction, minimized latency, and reduced switching noise level requiring innovative new methods for system integration. In contrast to common understanding, the space for electronic components in vehicles is very limited, so reduced electronic components count, and size are a must for the automotive industry as well. These applications and others have created a new era of printed circuit board (PCB) design transformation to system in package (SiP) design methodology. The need for SiP solutions has driven the entire semiconductor, packaging, design chain and supply chain industries to develop advanced technologies that can address the increasing needs for cost reduction, size reduction and performance enhancements for advanced electronic systems. The transition to SiP design requires new thinking, new approaches and solid methodologies for electronic circuit designs, components integration, assembly process and final testing as well as functional verifications. PCB design is based on horizontal component placement with sufficient distance to minimize electromagnetic coupling among passive components, pre-packaged Integrated Circuits, highly capacitive interconnect structures, and relatively easy to modify and enhance circuits. However, SiP designs are primarily based on vertical component placement, bare dice, and low capacitive interconnect structures to reduce power consumption. This presentation will describe the differences in the two approaches and explain the changes that are occurring to accomplish the transition.*  ***Nozad Karim, VP; SiP & Electrical Engineering, Amkor Technology*** *Nozad Karim presently is the Vice President of SiP & System Integration at Amkor Technology. He has over 30 years of experience working with semiconductor packaging, System in Package, circuit and system designs for digital, analog, and RF/Microwave applications. Prior to Amkor, he served in engineering and management roles with Motorola Communication, Texas Instruments, & Compaq/HP. Nozad Karin is a General Chair of IMAPS SiP Conference in USA and SiP Conference in China.*
9:30 am – 9:45 am	*BREAK IN THE FOYER SPONSORED BY:* INTEVAC

2018 IMAPS David Virissimo Spring Charity Golf Outing

A little fun in the sun THURSDAY afternoon…for a great cause!

	Interposers, 3D IC & Packaging *ROOM 104-106*	Fan-Out, Wafer Level Packaging & Flip Chip *ROOM 107-108*	Engineered Micro Systems/Devices *(including MEMS & Sensors)* *ROOM 102-103*
THURSDAY MORNING SESSIONS	THA1: DESIGN & SIMULATION Chairs: Inho Lee, Dow Electronic Materials; Prithwish Chatterjee, Intel Corporation	THA2: FLIP CHIP ASSEMBLY; EQUIPMENT AND MATERIALS Chairs: Islam Nokibul, STATSChipPAC; Kevin Martin, Atotech	THA3: ENGINEERED MICROSYSTEMS Chairs: Bruce Kim, City University of New York; Mike Kranz, EngeniusMicro
9:45 am – 10:15 am	019 Heterogeneous Integration: Are your design tools and methodologies up to the task? John Park, Cadence Design Systems	013 Lead Free Solder Plating Chemicals for Substrate Bumping Koji Tatsumi, Mitsubishi Materials Corporation (Daiki Furuyama, Mami Watanabe, Kyoka Susuki, Takuma Katase, Kiyotaka Nakaya, Masayuki Ishikawa)	041 Thermosonic Ball Bonding Recipe Optimization: Comparing Cu and PCC Wire on Two Pad Thicknesses Michael Hook, University of Waterloo (Michael Mayer, Stevan Hunter)
10:15 am – 10:45 am	016 Design, Characterization and Testing of Large-area and High-density 3D Interconnection by Direct Bond Interconnect Gill Fountain, Xperi (Rajesh Katkar, Michael Huynh, KM Bang, Bongsub Lee, Chandrasekhar Mandalapu, Guilian Gao, Thomas Workman, Gabe Guevara, Cyprian Uzoh, Laura Mirkarimi)	018 Advancement of Fine Pitch Interconnect Technology Nokibul Islam, StatsChipPAC Inc (Kang KeonTaek)	059 Electronic Packaging to Enhance IOT for Agricultural Applications Markus Kreitzer, Auburn University (R. Harrison, J. Craven, A. Muscha, R. N. Dean, E. A. Guertal)
10:45 am – 11:15 am	055 A System Co-Design Flow for 3D and Fan-out Package Architectures Narayanan TV, Zuken USA (Tom Whipple)	034 High-throughput Jetting in Micro-device Packaging Hanzhuang Liang, Nordson Asymtek	079 Instrumentation for Sensing Passive Eye Response due to Head Impact via MEMS IMUs Brent Bottenfield, Auburn University (Yuan Meng, Mark Adams)
11:15 am – 11:45 am		027 High Precision Uniquely Designed De-flux Cleaning Solution for Advanced Packaging Ajit Dhamdhere, Cactus Materials, Inc. (Ajit Dhamdhere, Wey Lyn Lee, Tofael Ahmed, Joaquin Santallin, Cactus Materials, Inc.; Takuro Jimbo, Suguru Kamikawaji, Kaken-Tech Co Ltd; Rafiqul Islam, Arizona State University)	056 Successful FPGA Obsolescence Form, Fit, and Function Solution Using a MCM and DER™ to Implement Original Logic Design Erick Spory, Global Circuit Innovations, Inc.

CONFERENCE ENDS BY 11:45 AM
FOUNDATION GOLF OUTING AT 1PM

SESSION NOTES:

(Be sure to use the ***MOBILE APP*** to download "extended abstracts"when you hear a presentation you like! ***Mobile APP sponsored in part by SETNA.)***

SESSION NOTES:

(Be sure to use the ***MOBILE APP*** to download “extended abstracts”when you hear a presentation you like! ***Mobile APP sponsored in part by SETNA.)***

SESSION NOTES:

(Be sure to use the ***MOBILE APP*** to download "extended abstracts"when you hear a presentation you like! ***Mobile APP sponsored in part by SETNA.)***

SESSION NOTES:

(Be sure to use the ***MOBILE APP*** to download “extended abstracts”when you hear a presentation you like! ***Mobile APP sponsored in part by SETNA.)***

Shaping the Future

Applied Materials is the leader in materials engineering solutions used to produce virtually every new chip and advanced display in the world. Our expertise in modifying materials at atomic levels and on an industrial scale enables customers to transform possibilities into reality. At Applied Materials, our innovations make possible™ the technology shaping the future.

Learn more: **www.appliedmaterials.com**

APPLIED MATERIALS®
make possible

Amkor Technology®

50 FIFTY YEARS
1968 - 2018

A proud legacy. An exciting future.

As the original pioneers of the OSAT industry, Amkor has helped define and advance the technology manufacturing landscape. Since 1968, we've delivered innovative packaging solutions with the service and capacity global customers rely on.

We're proud of what we've done, and can't wait to show you what's next.

www.amkor.com