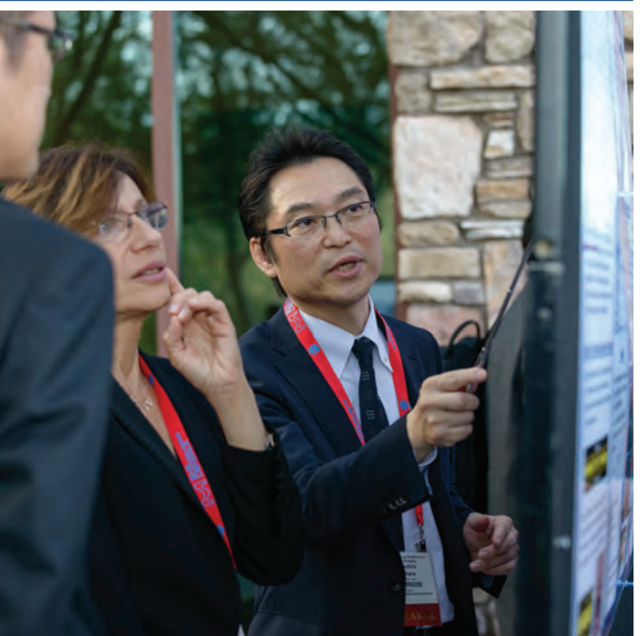
FINAL PROGRAM & EXHIBIT DIRECTORY

16th International Conference and Exhibition on

DEVICE PACKAGING

MARCH 2-5, 2020
We-Ko-Pa Resort | Fountain Hills, Arizona USA
www.imaps.org/devicepackaging



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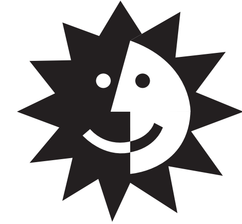

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MONDAY, MARCH 2:
9 Professional Development Courses (PDCs)
Welcome Reception: 5:30p-7:00p
TUESDAY, MARCH 3-THURSDAY, MARCH 5:
4 Keynotes - 2 Tuesday and 2 Thursday Morning
GBC Plenary Session Wednesday
Panel Discussion (Tues.) & Poster Session (Wed.)
Exhibits: 10a-630p (Tues.), 9:45a-4p (Wed.)

The SiP Company

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Package it.

Welcome to Device Packaging 2020!

Welcome to the 16th International Conference and Exhibition on Device Packaging (DPC 2020) -- the premier annual conference where the latest in microelectronics system integration and packaging technology is unveiled. This week's conference, organized by the International Microelectronics Assembly and Packaging Society (IMAPS), provides the stage to showcase the best in packaging technology available today, as well as those technologies soon to be released to the market. It offers the benefit of technical exchange among key international players and the opportunity to discover emerging business trends from top marketing analysts.

The conference provides a focused forum on the latest technological developments in three topical workshop tracks related to microelectronic packaging: ***3D Integration; Fan-Out, Wafer Level Packaging and Flip Chip***; and ***Advanced & Emerging Materials for Automotive, 5G & Next Generation Applications.***

The 2020 conference will feature four premier technical keynote speakers, a Global Business Council (GBC) plenary session on the ***ELECTRONICS INDUSTRY TRANSITION***, and twelve technical sessions featuring more than 60 technical presentations all covering the latest in packaging technology innovation. Attendees will also enjoy a poster session and happy hour, a selection of nine professional development courses, plus a sold-out vendor exhibition and technology showcase. Gather with your industry colleagues for networking receptions and gatherings throughout the week, including the welcome reception, the exhibit hall reception, the poster session and happy hour, and a charity golf outing.

We are very excited about the program we have put together this year. Several key topics in our industry are being addressed with our keynotes: ***HETEROGENEOUS INTEGRATION TECHNOLOGIES FOR MOORE'S LAW 2.0 AND BEYOND; RF FRONT END PACKAGING CHALLENGES IN 5G; INTEGRATED WAFER LEVEL PACKAGING TECHNOLOGIES FOR HIGH-PERFORMANCE COMPUTING SYSTEMS: CHALLENGES AND OPPORTUNITIES;*** and ***GET MOoRE OUT OF THE PACKAGE***.

Jan Vardaman from TechSearch and Beth Keser from Intel lead a panel discussion on Tuesday night on "***High Performance Computing: Are Chiplets the Answer?***".

We hope you find great value in DPC 2020 this week in Arizona. Be sure to take it all in - visit sessions, attend keynotes, speak with all of the exhibitors, and NETWORK as much as you can!

Please utilize the mobile APP from your phone or tablet or visit www.imaps.org/devicepackaging for more updates. Contact IMAPS staff if you need any assistance.

JCET

Booth 20

www.jcetglobal.com

Program at a Glance

Monday, March 2:

Registration: 7:00 am - 7:00 pm
Professional Development Courses (PDCs): 10:00 am - 5:30 pm
WELCOME RECEPTION: 5:30 pm - 7:00 pm

MORNING Professional Development Courses (PDCs) – **10:00am-12:00pm**			
PDC1: Introduction to Fan-Out Packaging *CANCELLED*	PDC2: *ROOM 102* System-in-Package (SiP) System Solutions Through Miniaturization Course Leader: Mark Gerber, ASE US, Inc	PDC3: *ROOM 104* Basics of Conventional and Advanced Chip Packaging Course Leader: Syed Sajid Ahmad	
LUNCH (boxed lunches can be picked up in the foyer from 12-12:30pm) *Only provided for those attendees registered for BOTH Morning and Afternoon PDCs*			
EARLY AFTERNOON Professional Development Courses (PDCs) – **1:00pm-3:00pm**			
PDC4: *ROOM 103* Development of Advanced Fan Out Technologies Course Leader: John Hunt, ASE US, Inc.	PDC5: *ROOM 102* 3D Package Assembly and Technology for Mobile Devices Course Leader: Tom Dory, Fujifilm Electronics Materials	PDC6: *ROOM 104* Gold-Aluminum Intermetallics Course Leader: Syed Sajid Ahmad	PDC7: *ROOM 105* Fundamentals of 5G Course Leader: Ivan Ndip, Fraunhofer IZM
COFFEE BREAK IN FOYER			
LATE AFTERNOON Professional Development Courses (PDCs) – **3:30pm-5:30pm**			
PDC8: *ROOM 103* Advances in Fan-Out Wafer Level Packaging (FOWLP) Course Leader: Beth Keser, Intel Corporation	PDC9: *ROOM 102* The Evolution of Flip Chip Package Technology Course Leader: Mark Gerber, ASE US, Inc	PDC10: *ROOM 104* Polymers in Wafer Level Packaging Course Leader: Jeffrey Gotro, InnoCentrix, LLC	PDC11: 5G/mmWave Package Development Requirements and Solutions *CANCELLED*

Tuesday, March 3

7:00 am - 7:00 pm
Registration

8:00 am - 9:55 am
Opening & Keynote Presentations
(ROOM 107-108)

10:00 am - 6:30 pm
Exhibits Open
(Wasaja Ballroom)

10:30 am - 12:30 pm
Technical Sessions – T-AM1-T-AM3

12:30 pm - 2:00 pm
Lunch Break In Exhibit Hall

2:00 pm - 5:30 pm
Technical Sessions – T-PM1-T-PM3

5:30 pm - 6:30 pm
Reception In Exhibit Hall
(Wasaja Ballroom)

6:30 pm - 8:00 pm
Evening Keynote & Panel Session on:
HIGH PERFORMANCE COMPUTING: ARE CHIPLETS THE ANSWER?
(ROOM 107-108)

Wednesday, March 4

7:00 am - 6:00 pm
Registration

8:00 am - 12:00 pm
GBC Keynote & Plenary Session on
ELECTRONICS INDUSTRY TRANSITION
(ROOM 107-108)

9:45 am - 4:00 pm
Exhibits Open
(Wasaja Ballroom)

12:00 pm - 1:30 pm
Lunch Break In Exhibit Hall

1:30 pm - 5:30 pm
Technical Sessions – W-PM1-W-PM3

5:30 pm - 6:30 pm
Poster Session & "Happy Hour"
Outside on Patio/Grass

6:30 pm - 7:30 pm
2020 3D InCites Awards Ceremony and "Bonus Happy Hour"
Hosted by IMAPS

Thursday, March 5

7:00 am - 11:30 am
Registration

8:00 am - 9:30 am
Keynote Presentations
(ROOM 107-108)

9:45 am - 11:45 am
Technical Sessions – TH-AM1-TH-AM3

11:45 am
Conference Ends

1:30 pm - 7:00 pm
IMAPS David Virissimo Memorial Spring Charity Golf Outing

Separate Registration - See Website or contact IMAPS Staff if you are interested to tee it up for a good cause!
WeKoPa Golf Club
1:30 pm Shotgun Start
"Scramble"

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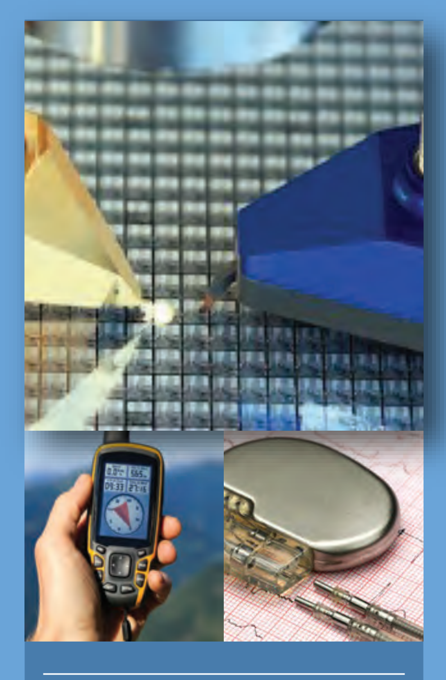

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Access the Device Packaging *MOBILE APP*

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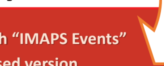

The mobile app is the exclusive source for all speaker abstracts, PLUS:

- The *full* conference program
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- Searchable exhibitor list
- Info, Links, and News
- Conference updates and changes
- Personal conference schedule

Here's how to get the app

1. Visit the Apple Store or the Google Play store and search "IMAPS Events" or visit https://imaps.gatherdigital.com for the web-based version.
2. Log in with your registration email and the password dpc2020.
3. Take advantage of all of the attendee and exhibitor features!

Device Packaging Exhibition and Technology Showcase
Exhibiting Companies

The exhibit hall is now ***SOLD OUT, marking this the 15th consecutive year of a sellout, and with more than 10 companies on a waitlist!*** The following booths will be on display during Device Packaging 2020. Please visit the companies' websites listed below for more information. The floor plan of the exhibit hall is included on the following page as well. If you have questions about exhibiting with IMAPS, or about getting signed up for the Device Packaging Conference Exhibitions, contact Brian Schieman at bschieman@imaps.org

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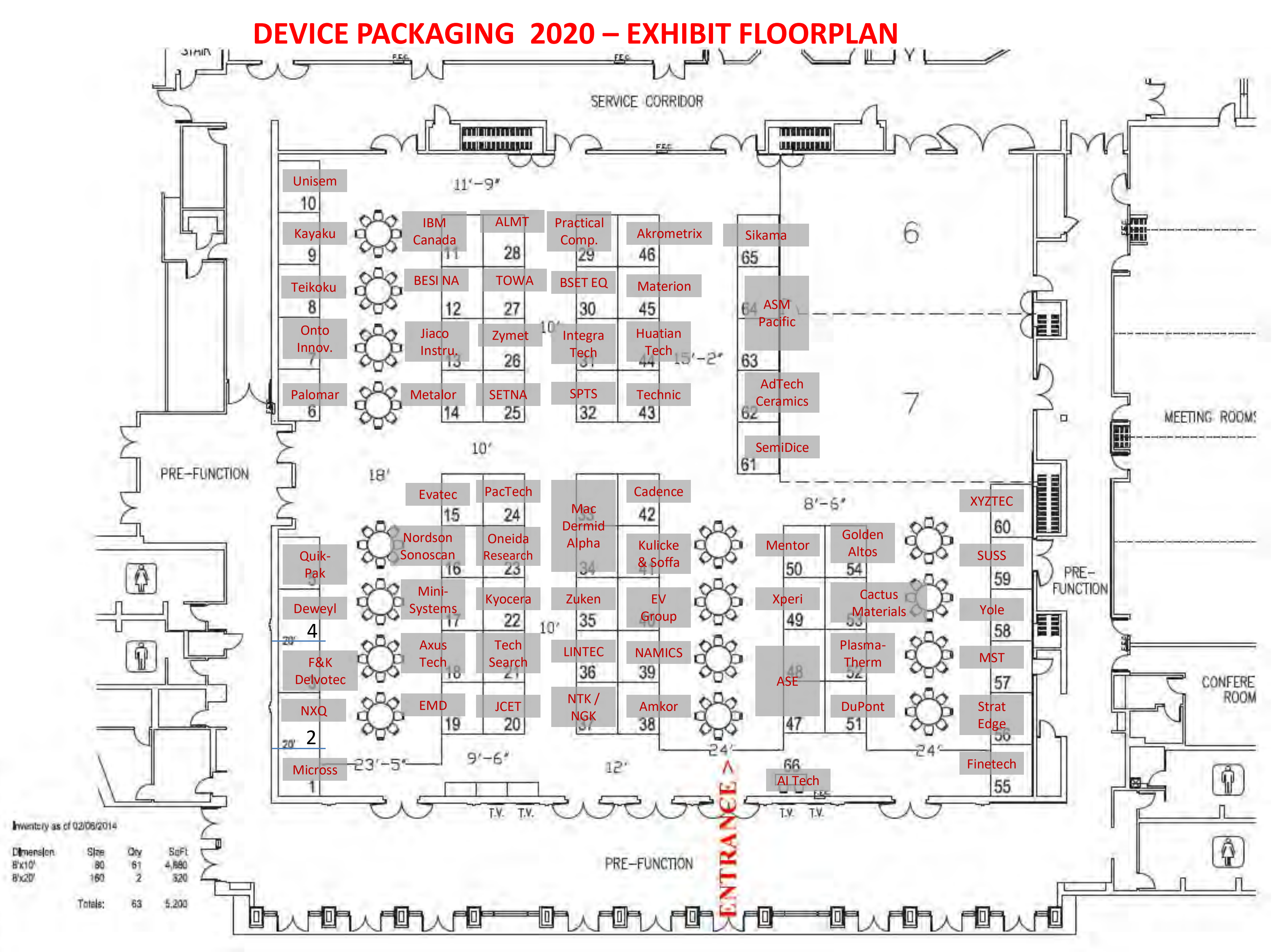
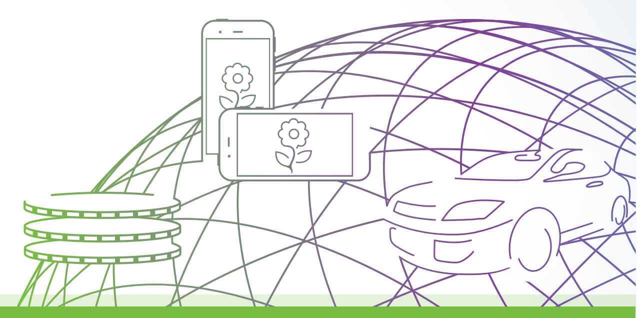
DEVICE PACKAGING 2020 – EXHIBIT FLOORPLAN





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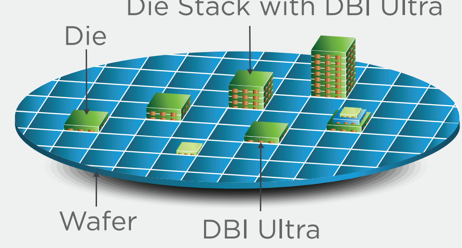

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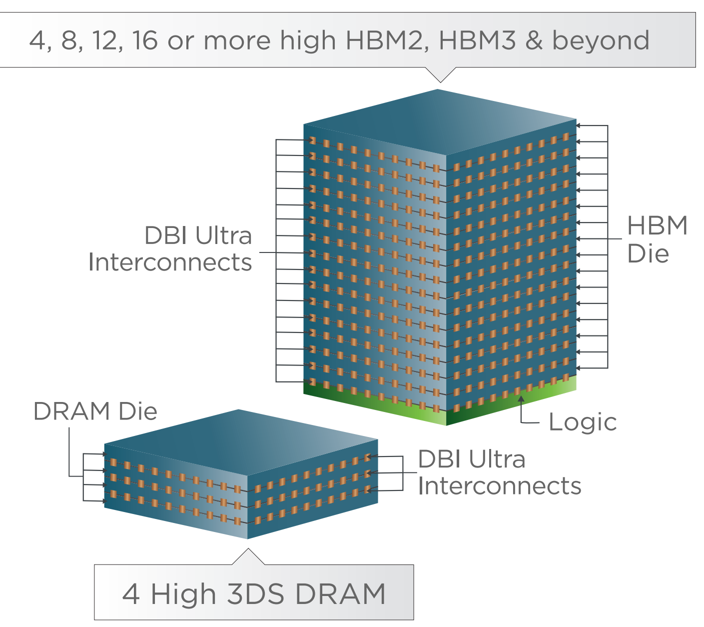

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Enabling Next Generation High Permanence Computing

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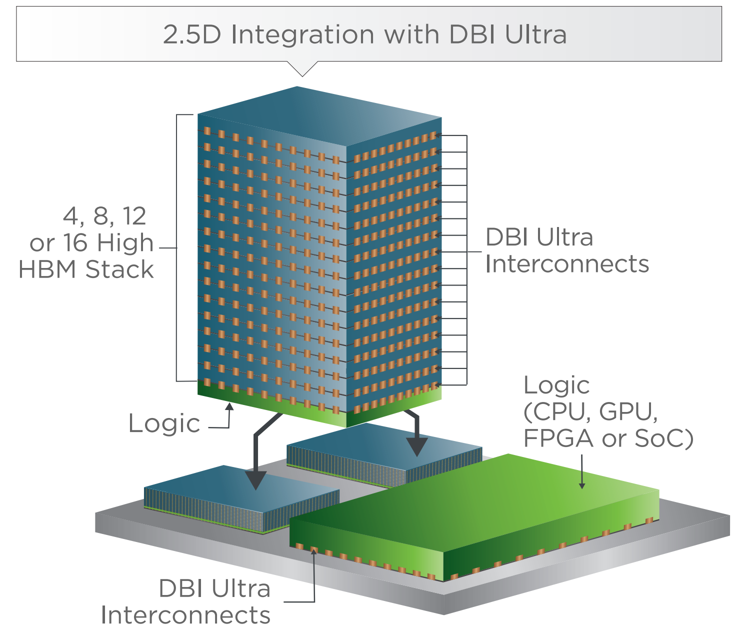

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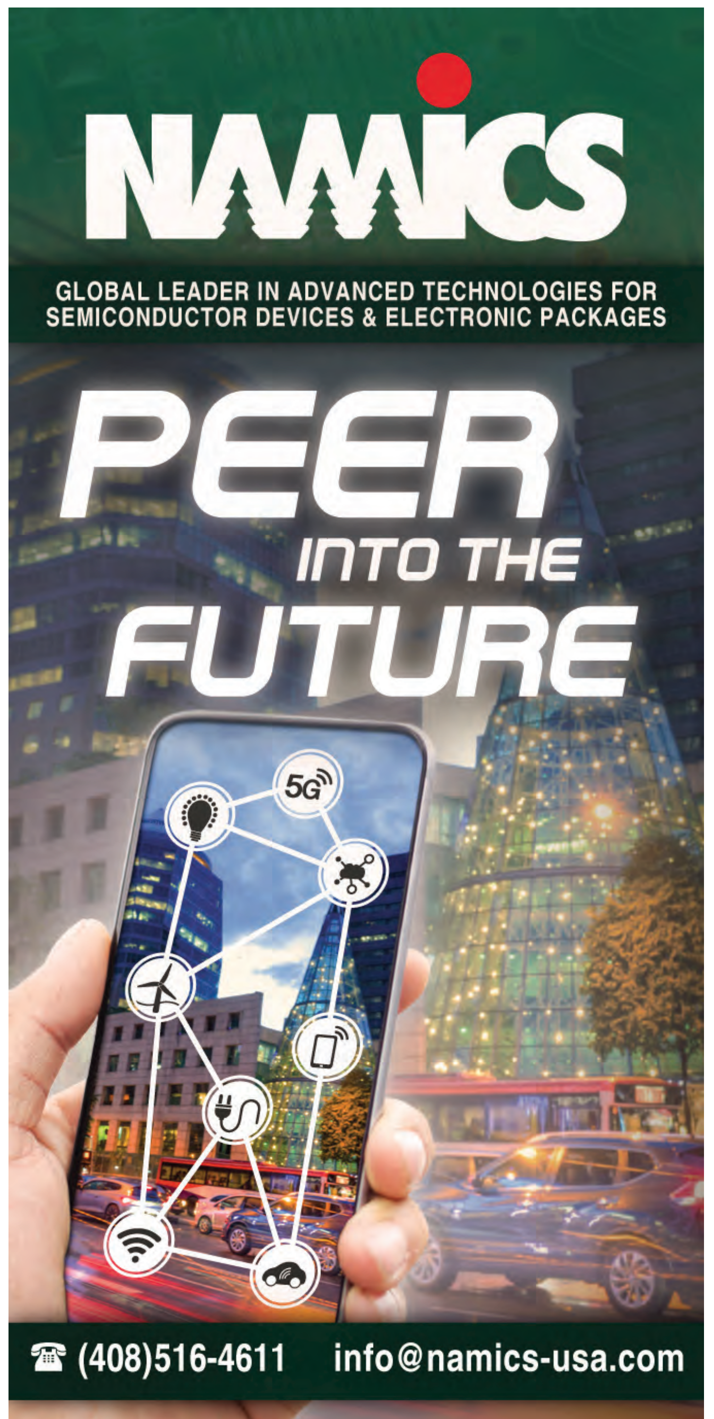

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Booth: 28

A.L.M.T. Corp.

Tokyo, Japan
www.allied-material.co.jp/en.html

We, A.L.M.T. Corp., are one of the biggest manufacturers of tungsten, molybdenum and diamond-based heatspreader , located in Japan, Sumitomo Electric Group. From raw materials to processed products, we are working on developing various kinds of new materials.

Booth: 62

AdTech Ceramics

Chattanooga, TN USA
www.adtechceramics.com

AdTech Ceramics is a fully integrated US based manufacturer of high temperature co-fire ceramic (HTCC) electronic packages and precision injection molded ceramic components. Standard ceramic materials offered include multilayer aluminum oxide and aluminum nitride. AlN is often preferred due to its excellent thermal conductivity and desirable coefficient of thermal expansion. AdTech also produces chemically or CNC milled metal components including package lids, leads and seal rings. Our injection molded products can be provided as fired, with metallization and plating or as full ceramic-to-metal assemblies. In our continuous drive for innovation and advanced technology for our growing customer base, we have recently added copper thick film metallization on alumina or aluminum nitride and ENEPIG plating capabilities. Located in Chattanooga, TN and with over 45 years of experience producing multilayer ceramic packages, we are ideally positioned to take on your most challenging package designs. Originally established as American Lava in 1903, AdTech has been owned by 3M, GE and Coorstek prior to is becoming Advanced Technical Ceramics Company in 2004. AS9100D/ISO9001:2015 certified and NADCAP accredited.

Booth: 66

AI Technology, Inc.

Princeton Junction, NJ USA
www.aitechnology.com

AI Technology, Inc. (AIT) developed flexible epoxies for microelectronic packaging in 1985. Today, AIT's product line includes patented component, substrate and large die bonding adhesives and underfills, stack-chip packaging with dicing die-attach film (DDAF), flip-chip bonding and underfilling, single and multiple-chip module die bonding (230°C and above), and component and substrate bonding adhesives for military and commercial applications. AIT's thermal interface materials, including phase-change pads, greases, gels and adhesives, ensure ultimate performance in semiconductors, modules, computers and communication electronics applications.

Booth: 46

Akrometrix

Atlanta, GA USA
www.akrometrix.com

Akrometrix is the worldwide leader of PCB and component thermal warpage metrology systems and test services utilizing Digital Fringe Projection (DFP), Shadow Moiré, and Digital Image Correlation (DIC) technologies utilized by various types of customers within the electronics industry. Our systems measure "at-room-temperature" warpage, thermal warpage [-50°C to 350°C], and thermal strain of substrates, materials, and electronic components/ assemblies at critical reflow temperatures. Akrometrix systems provide graphical, statistical, and tabular results in order to help our customers comply to various industry standards.

Booth: 38

Amkor Technology, Inc.

Tempe, AZ USA
www.amkor.com
Twitter: https://twitter.com/AmkorTechnology

Amkor Technology is one of the world's largest providers of outsourced semiconductor packaging and test services and a strategic manufacturing partner to leading semiconductor companies, foundries and electronics OEMs. Founded in 1968, Amkor's operational base includes production facilities, product development centers and sales and support offices in Asia, Europe and the USA. Amkor's broad package portfolio includes leadframe, FCBGA, fcCSP and WLCSP products. MEMS, sensors and SiP packaging with unique development and high-volume production requirements are also supported. Amkor's MicroLeadFrame® (MLF®) and ChipArray® BGA packages have become industry standards as QFNs and FBGAs. Large scale and complex 2.5/3D system solutions are supported using High-Density Fan-Out (SWIFT®) technology. Amkor also provides high volume copper pillar bumping and Package-on-Package (PoP) assemblies found in many smart mobile products. Services include package design and development, wafer probe and package test, wafer bumping and redistribution, package assembly and final test. Engineering services offer best-in-class thermal, electrical and mechanical modeling and characterization as well as design automation. Test engineering services range from test program development to full product characterization of packaged RF, mixed signal, logic and memory devices. As the provider of choice for semiconductor assembly and test, Amkor offers comprehensive manufacturing capability and scale along with a broad global presence. Visit www.amkor.com

Booth: 47-48

ASE Group

Santa Clara, CA USA
www.aseglobal.com
Twitter: @asegroup_global

Alongside a broad portfolio of established technologies, OSAT industry leader ASE is also delivering innovative advanced packaging and System-in-Package solutions to meet growth momentum across a broad range of end markets. For more about our advances in SiP, Fanout, WLP, MEMS, Flip Chip, and, 2.5D, 3D & TSV technologies, all ultimately geared towards applications to improve lifestyle and efficiency, please visit: www.aseglobal.com.

Booth: 63-64

ASM Pacific Technology

Tempe, AZ, USA
www1.asmpacific.com/en/

ASM Pacific Technology is the World Leader in Advanced Packaging Equipment Solutions, SMT Equipment, and Lead frame Materials. With a vision of providing customer focused cost effective solutions, we offer IC Assembly, Opto-electronic, Electronic Manufacturing, Physical Vapor Deposition / Chemical Vapor Deposition Equipment and Lead frame technology that is in the forefront of the Semiconductor Equipment Industry. ASMPT is the only IC Assembly Equipment provider recognized as one of 2019 Thomson Reuters Top 100 Global Technology Leaders.

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Axus Technology

Chandler, AZ USA
www.AxusTech.com

Axus Technology is a highly specialized technology supplier focused on engineering capability and efficiency to provide CMP, wafer cleaning and precision wafer grind process consulting services to emerging technology industries including MEMS, Automotive, Defense and Aerospace, Lifesciences and IoT as well as traditional semiconductor processing. The highly experienced Process Development team facilitates advances in wafer technology and efficient wafer production with new designs and novel applications. Based in Chandler, Arizona, Axus Technology operations include a fully-equipped class 100 foundry cleanroom for development and foundry processing, as well as design, manufacturing, and worldwide service and parts support for existing equipment including over 6000 line items of CMP and grinder parts.

Booth: 12

Besi North America, Inc

Chandler, AZ USA
www.besi.com

Besi develops and supplies leading edge semiconductor manufacturing systems offering high levels of accuracy, reliability and productivity. Besi's primary products include die attach systems (epoxy, flip chip, TCB and Hybrid Bonding), packaging equipment (including molding, saw Singulation and trim and form), and plating systems.

Booth: 30

BSET EQ

Antioch, CA USA
www.bseteq.com

BSET EQ designs and manufactures Gas Plasma Systems Used for Plasma Etching, Plasma Cleaning, Plasma Surface Treatment and Plasma IC Decapsulation for Failure Analysis and IC Counterfeit Detection. These dry processes are environmentally friendly and our systems are used worldwide in an increasing number of industries. BSET EQ is also the exclusive North American distributor for ATV Technologie GmbH IR Vacuum Solder Reflow Ovens and Thermal Processing Systems. These systems range from small tabletop systems to High Volume Automated Vacuum Reflow Systems. The product range also includes Sintering Presses, High Vacuum Getter Activation systems, Atomic Layer Deposition systems and Diamond Scribers. BSET EQ has your Plasma and Thermal Solution.

Booth: 53

Cactus Materials, Inc

Tempe, AZ, USA
www.cactusmaterials.com

Cactus Materials provides process development services in Wafer Bonding, Through-Silicon Via (TSV), 3D Integration, and Thin Film Synthesis. Our expertise in wafer bonding allows us to produce a high throughput without the need for ultra-high vacuum. Our process allows for spontaneous room temperature bonding and batch annealing below 200C. The types of bonding we can do are Si-based bonding, hybrid bonding, heterogeneous bonding, and temporary bonding. Besides that, Cactus Materials offers Low Temperature Co-Fired Ceramic (LTCC) materials and packages for RF modules with excellent performance characteristics for a wide range of packaging applications including conductors with low electrical resistance and dielectrics with high flexural strength in multi-layer and mono-layer structures. This has applications in high speed wireless data communications, wireless modules, power amplifier modules, etc.

Booth: 42

Cadence

San Jose, CA USA
www.cadence.com
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Cadence enables electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work, and play. Cadence software, hardware, and semiconductor IP are used by customers to deliver products to the market faster. The company's Intelligent System Design strategy helps customers develop differentiated products—from chips to boards to Intelligent systems—in mobile, consumer, cloud, data center, automotive, aerospace, IoT, industrial, and other market segments. Cadence is listed as one of Fortune Magazine's 100 Best Companies to Work For. Learn more at www.cadence.com.

Booth: 4

DeWeyl Tool Company, Inc.

Petaluma, CA USA
www.deweyl.com

DeWeyl provides the finest quality bonding wedges in the world. Located in the Petaluma, CA, DeWeyl's primary business is manufacturing wire bond wedges and custom high precision tooling for the semiconductor, aerospace and medical industry. DeWeyl produces wedges made from ceramic, titanium and tungsten carbide for small and large round wire and ribbon applications.

Booth: 51

DuPont

Marlborough, MA USA
www.dupont.com

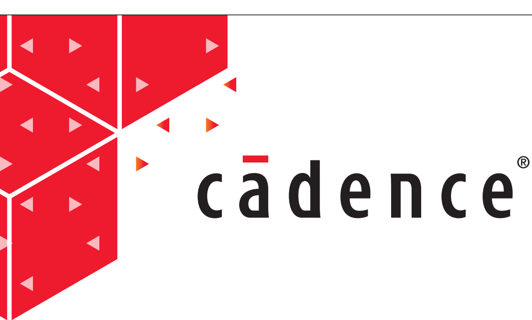
DuPont Electronics & Imaging uses industry-leading technologies to enable smaller, smarter and faster electronics, transform the sun's rays into clean energy, and bring high-quality printing to packaging and textiles.

Booth: 19

EMD Performance Materials Corp

San Diego, CA USA
www.emdgroup.com

EMD Performance Materials is a business of Merck KGaA, Darmstadt, Germany. Our Semiconductor Solutions business unit accelerates the semiconductor industry to develop electronic devices that are smarter, faster, more powerful & energy efficient for a more connected world. We provide highly innovative material-based solutions for the semiconductor manufacturing supply chain. From wafer fabrication towards the final stage, packaging – we are a single channel partner for the production of integrated circuits. Focusing on packaging only, we e.g. offer a variety of Thick Film Resists (TFR) from conventional DNQ & chemically amplified (CA) positive tone to photo polymerizing negative tone which are used to make patterned conductive circuitry in semiconductor packages. In addition we deliver high reliability and environmentally friendly interconnect materials to enable powerful semiconductors that are fully lead-free and ROHS compliant. When great minds get together, they inspire each other. We are proud to partner with IMAPS again in 2020 to further accelerate innovation in Semiconductors.



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Booth: 15

Evatec

Trübbach, Switzerland
www.evatecnet.com

Evatec delivers complete thin film production solutions for Advanced Packaging. From HEXAGON delivering FOWLP with the lowest Rc of < 1mOhm, the longest etch kit life and highest wafer throughput, to the CLUSTERLINE PNL for FOPLP and IC substrate manufacturing on substrate sizes of 650mm, we offers proven production solutions at wafer and panel level. For chip level EMI shielding our know how in soft magnetics, multi layer stack deposition with close management of temperature and high speed handling are combined on SOLARIS for a high throughput, compact platform with a low CoO. To find out more about Evatec thin film production solutions across all our markets of Advanced Packaging, Semiconductor, Optoelectronics and Photonics visit www.evatecnet.com. Alternatively call our local office in North America on +1 727 201 4313

Booth: 40

EV Group

Tempe, Arizona, US
www.evgroup.com

EV Group (EVG) is a leading supplier of equipment and process solutions for the manufacture of semiconductors, microelectromechanical systems (MEMS), compound semiconductors, power devices, and nanotechnology devices. Key products include wafer bonding, thin-wafer processing, lithography/nanoimprint lithography (NIL) and metrology equipment, as well as photoresist coaters, cleaners and inspection systems. Founded in 1980, EV Group services and supports an elaborate network of global customers and partners all over the world. More information about EVG is available at www.EVGroup.com.

Booth: 3

F&K Delvotec

Foothill Ranch, CA, USA
www.fkdelvotecusa.com

F&K Delvotec is a leader in Wire Bonding, with innovations in ball bonding, fine and large-wire wedge bonding, and laser bonding. Delvotec offers a range of working areas, including large-area bonders for batteries and large panels. Delvotec's new Laser Bonder makes exceptionally strong bonds with a wide variety of ribbons and surfaces.

Booth: 55

Finetech

Gilbert, AZ, USA
www.finetechusa.com

Finetech supplies sub-micron accuracy die bonders for die attach, advanced packaging and micro assembly applications. Manual, motorized and automated models provide a pathway from prototyping to production. These modular systems allow high process flexibility with a wide range of controlled bonding forces. Bonding technologies include thermo-compression, ultrasonic, eutectic, epoxy, sintering, ACF/ACP, Indium and precision vacuum die bonding. Applications areas cover optical packages, sensors, Si photonics, microLEDs, MEMS, Cu pillar, focal plane arrays, chip-on-glass, chip-on-flex and more. The deep process knowledge we have gained through decades of experience adds value to our equipment. Our engineers work with customers to create effective solutions for specific applications - they understand that "one size" does not necessarily fit all.

Booth: 54

Golden Altos Corporation

Milpitas, CA USA
www.goldenaltos.com

If you're looking for turnkey monolithic or hybrid assembly, fully compliant qualifications, complete burn-in services or any stage in between, you've found your answer. At Golden Altos, we're committed to providing the semiconductor, military and aerospace communities with quality service building both single chip and multichip modules.Quality isn't just a word at Golden Altos. We continually strive to deliver the finest products, services and documentation. We do this through our own internal quality system as well as regular certifications through outside and government agencies.

Booth: 44

Huatian Technology Group

Phoenix, AZ USA
www.flipchip.com

FCI-HT supplies turnkey semiconductor assembly and test services to the consumer, automotive, industrial and medical industries. FCI-HT supports a wide range of customers, frequently partnering with them to engineer customized solutions including expedite bumping and backend services on Multi-Project Wafers. FCI-HT is a leader in wafer level packaging with patented technologies spanning from Cu Pillar Bumping, Spheron™ Wafer Level Chipscale Packaging, and ChipsetT™ Embedded Die Packaging. FCI-HT is a division of Huatian Technologies (HT). HT is among the top 6 OSATs in the world with over one billion dollars in annual revenue. It is listed on the Shenzhen Stock Exchange Market. Huatian has six ISO/TS16949 factories located in the US and China offering a complete range of semiconductor packaging and turnkey services.

Booth: 11

IBM Canada Ltd

Bromont, Quebec, Canada
www.ibm.com/assembly

IBM Bromont is a world leader in semiconductor packaging technology, products and services. Now available to customers worldwide, we invite you to take advantage of our experience, system level mindset, and skilled engineers to execute your most advanced packaging and test solutions. Tap into our deep competencies as the industry continues to shift to custom SoCs and SiPs. IBM is known for its multi-chip packaging and heterogeneous integration. We offer full turnkey solutions from modelling and characterization through Burn-in and test. Our test capability spans digital, analog, mixed signal, RF as well as multi-site programming, test pattern conversion, and load board design. We provide high quality mechanical, thermal and electrical design (including high speed/SERDES, signal integrity and power integrity), ensuring effective execution of new and updated platforms. Services include materials and process characterization, optimized substrate design, and failure analysis while package platforms range from large organic substrates to high density interconnect substrates such the 2.1D and 2.3D technologies. We invite you to discuss your next generation requirements – our developments in areas such as silicon photonics are unrivaled. IBM will help you deliver differentiated solutions while providing personalized, expert support to meet even the toughest application goals.

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Booth: 31

Integra Technologies, LLC

Milpitas, CA USA
www.integra-tech.com

Integra Technologies is a global leader in the sourcing, packaging, testing and characterization of highly specialized, mission-critical semiconductor components and related value-added services for high-reliability ("Hi-Rel") applications where dependability and failure-free performance are of paramount importance.

Integra provides a span of in-house services and capabilities to support a broad variety of Hi-Rel components throughout the entire value-added life-cycle - from prototyping, through testing, and ultimately to volume production. More specifically, Integra specializes in semiconductor die prep, packaging, assembly, test, reliability qualification, DPA and FA service for high-reliability applications.

Booth: 20

JCET

Fremont, CA USA
www.jcetglobal.com

JCET Group is a leading global semiconductor packaging and test provider, offering a full range of turnkey services that include semiconductor package design and characterization, R&D, wafer probe, wafer bumping, package assembly, final test and drop shipment to vendors around the world. Our comprehensive portfolio covers a wide spectrum of semiconductor applications including mobile, communication, compute, consumer, automotive and industry etc., through advanced wafer level packaging, 2.5D/3D, System-in-Package, flip chip and wire bonding technologies. JCET Group has three R&D centers, six manufacturing locations in China, Singapore and Korea, and sales centers around the world providing close technology collaboration and efficient supply-chain manufacturing to customers in China and throughout the world. For more details please visit www.jcetglobal.com

Booth: 13

JIACO Instruments

Delft, Netherlands
www.jiaco-instruments.com

Visit JIACO Instruments at booth #13 to discuss damage free decapsulation. JIACO Instruments Microwave-Induced-Plasma decapsulation is the new standard for reliable Reliability Test & Failure Analysis. The fully automated decapsulation process is highly selective; critical failure sites in advanced packages e.g. SiP, WCLSP, automotive are retained without process induced damage to challenging materials e.g. Ag, Cu bond wire, GaAs, Cu RDL, BOAC.

The JIACO Instruments MIP system has been in the market since mid-2016 and is now in use by many renown global companies for reliable failure analysis and quality control.

Booth: 9

Kayaku Advanced Materials, Inc.

Westborough, MA USA
www.kayakuAM.com

Kayaku Advanced Materials, Inc. (formerly MicroChem), a wholly owned subsidiary of Nippon Kayaku Co. Ltd., is a manufacturer of specialty electronic materials, providing innovative chemical solutions to MEMS, microelectronic and semiconductor markets. It specializes in photoimageable epoxy; e-beam, bi-layer lift-off & dielectric resists; and a suite of ancillary lithography products, as well as plating & RDL materials for advanced packaging. Additionally, Kayaku Advanced Materials' product lines include Applied Ink Solutions functional printed electronic inks & coatings; and Paratronix parylene conformal coating services & equipment sales. Kayaku Advanced Materials also has an exclusive licensing and distribution partnership with DuPont Electronic Materials for DuPont, Shipley semiconductor & advanced packaging electronic materials.

Booth: 41

Kulicke and Soffa Industries

Fort Washington, PA USA
www.kns.com

Kulicke & Soffa is a leading provider of semiconductor packaging and electronic assembly solutions supporting the global automotive, consumer, communications, computing, and industrial segments. As a pioneer in the semiconductor space, K&S has provided customers with market leading packaging solutions for decades. In recent years, K&S has expanded its product offerings through strategic acquisitions and organic development, adding advanced packaging, electronics assembly, wedge bonding and a broader range of expendable tools to its core offerings. Combined with its extensive expertise in process technology and focus on development, K&S is well positioned to help customers meet the challenges of packaging and assembling the next-generation of electronic devices.

Booth: 22

Kyocera Internaional, Inc.

San Diego, CA, USA
https://americas.kyocera.com/sc/

Kyocera Semiconductor Components Group offers a wide selection of semiconductor packaging technologies for medical equipment, database/servers, automotive, wireless/optical communication and consumer electronics industries. Technologies range from PCB and high density organic substrates to ceramic multilayer packages to epoxy molding compounds and die attach pastes. The combination of Kyocera's advanced material technologies, manufacturing processes and extensive design capabilities allow us to offer high-quality package and service solutions to meet the needs of our customers across a wide range of industries.

Booth: 36

LINTEC OF AMERICA, INC.

Phoenix, AZ USA
www.lintec-usa.com

LINTEC of AMERICA INC. Advanced Technologies Division 15930 S. 48th Street Suite 110 Phoenix, AZ 85048 Phone: 480-966-0784 Website: www.lintec-usa.com LINTEC is a worldwide leader in adhesive technologies. For 30+ years, LINTEC has created equipment and materials to solve difficult semiconductor process issues. With a catalog of hundreds of tapes and equipment, and decades of application experience, LINTEC is positioned to help. Whether you are looking for tape, need equipment to mount, peel or UV cure - our staff stands ready to assist you to provide the Adwill Advantage.

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Booth: 33-34

MacDermid Alpha Electronics Solutions

Waterbury, CT USA
www.MacDermidAlpha.com
Twitter: @MacDermidAlpha

Through the innovation of specialty chemicals and materials under our Alpha, Compugraphics, and MacDermid Enthone brands, MacDermid Alpha Electronics Solutions provides solutions that power electronics interconnection. We serve all global regions and every step of device manufacturing within each segment of the electronics supply chain. The experts in our Semiconductor Solutions, Circuitry Solutions, and Assembly Solutions divisions collaborate in design, implementation, and technical service to ensure success for our partner clients. Our solutions enable our customers' manufacture of extraordinary electronic devices at high productivity and reduced cycle time. Find out more at MacDermidAlpha.com.

Booth: 45

Materion

Buffalo, NY, USA
www.materion.com
Twitter: https://twitter.com/materioncorp

Materion is an industry leader in providing durable and best-cost solutions for ceramic packages and hermetic cover/lids for the microelectronics industry. We offer a comprehensive portfolio of packaging materials in precious or non-precious metals, and we can customize innovative electronic package materials to satisfy your needs. Our high-reliability packaging also supports most configurations, applications and volume requirements. Because of our industry expertise, extensive global manufacturing capabilities, and R&D proficiency, we are able to meet customers' packaging requirements today and partner with them to meet future challenges.

Booth: 50

Mentor, A Siemens Business

Wilsonville, OR USA
www.mentor.com/pcb

Mentor, A Siemens Business is the worldwide market leader in PCB systems design, advanced IC Packaging solutions and analysis technologies. Mentor, A Siemens Business will be showcasing its Xpedition High Density Advanced Packaging (HDAP) prototyping, design and verification solutions for heterogeneous multi-substrate designs such as FO-WLP, 2.5D and system-in-package. Visit booth #50 to learn more about Mentor's technologies and best practices for IC/Package/Board co-design.

Booth: 14

Metalor

North Attleboro, MA USA
www.metalor.com

Metalor's Advanced Coatings Division is uniquely positioned as the only global source of precious metal commodities and plating solutions with manufacturing sites and refineries throughout US, Asia, and Europe. Our comprehensive plating process range includes precious metal solutions and ancillary products. Metalor offers gold, silver, platinum, palladium, rhodium, ruthenium materials designed for use in semiconductor, electronic, and decorative applications. We offer a complete service; the supply of precious metal replenishment salts and anodes, process chemistry, as well as refining services can be your one-stop provider for precious metal needs. Our Technical Service Team, located facilities worldwide, is on call and equipped to provide rapid response to specific customer queries as well as on-site installation support.

Booth: 57

Micro Systems Technologies, Inc.

Lake Oswego, OR, USA
www.mst.com
Twitter: https://twitter.com/microsystemstec

The MST group is specialized in developing and manufacturing miniaturized, integrated electronic module solutions. The capabilities include highly complex HDI/microvia PCBs, semiconductor packaging processes as well as advanced assembly in the field of SMT and chip & wire.

Booth: 1

Micross

Orlando, FL USA
www.micross.com
Twitter: @microsscomps

Micross invites you to visit us at IMAPS Device Packaging, Booth 1. Micross will be showcasing multiple advanced interconnect and assembly technologies facilitating next-generation electronic systems, including wafer level packaging processes for solder (Pb-based and Pb-free) and Cu pillar bumping, high density (fine pitch) interconnects, through silicon vias (TSV) and silicon and glass interposers. These capabilities support a breadth of 2.5 and 3D heterogeneous integration packaging options as well as provide unique solutions to commercial, private, and government customers for their most challenging interconnect and packaging requirements. Whether there is a need to process a single wafer or if you are looking for a source to provide recurring production services, Micross offers full in-house wafer bumping solutions and a wide array of WLP technologies. In business for 40+ years, Micross' comprehensive array of high-reliability capabilities serves the global defense, space, medical, industrial and fabless semiconductor markets. Micross is the leading one-source provider of bare die & wafers, wafer bumping & advanced interconnect technologies, custom packaging & assembly, component modification services, electrical & environmental testing and Hi-Rel products to manufacturers and users of semiconductor devices. Learn more: Visit micross.com or email: onesource@micross.com

Booth: 17

Mini-Systems, Inc.

N Attleboro, MA USA
www.mini-systemsinc.com

Mini-Systems, Inc. (MSI) has over 45 years of proven as a one of worldwide leader in manufacturing high precision, high reliability passive components and high performance electronic packages. Thick Film and Thin Film Divisions offer wide range selection of thin film and thick film chip resistors along with capacitors. Package Division offers the varieties of hermetic sealed packages operating from DC to 40+ GHz. ISO9001 registered. RoHS compliant products available.

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Booth: 39

NAMICS Corporation

San Jose, CA USA
www.namicsusa.com

NAMICS is a global technology leader for underfills, encapsulants, adhesives, and insulating and conductive materials used by producers of semiconductor devices, passive components and solar cells with over 70 years of experience and expertise. Headquartered in Niigata, Japan with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea, Hong Kong, and China, NAMICS serves its worldwide customers with enabling products for leading edge applications. We build more than products; we build relationships setting the gold standard for customer service by offering customizing products, world class customer support to provide a solution for your personal application.

Booth: 16

Nordson SONOSCAN

Elk Grove Village, IL USA
www.nordsonsonoscan.com

Founded in 1973 and headquartered in Chicago, IL, Nordson SONOSCAN is a worldwide leader and innovator in Acoustic Micro Imaging (AMI) technology. Nordson SONOSCAN manufactures and markets acoustic microscope instruments and accessories to nondestructively inspect and analyze products. Our C-SAM scanning acoustic microscope provides unmatched accuracy and robustness setting the standard in AMI for the inspection of products for hidden internal defects such as poor bonding, delaminations between layers, cracks and voids. In addition, Nordson SONOSCAN offers analytical services through regional testing laboratories in the U.S., Asia and Europe and, educational seminars for beginners to advanced users on AMI technology. Some of our facilities also include X-ray inspection capability using Nordson DAGE Quadra systems.

Booth: 2

NXQ

Morgan Hill, CA, USA
www.nxqinc.com

Neutronix-Quintel (NXQ) is a leading provider of high performance mask alignment systems since 1978. NXQ is comprised of a team of seasoned industry veterans with vast experience in photolithography, providing their customers with the most robust solutions which have been refined over many years of customer driven innovations. NXQ has well over 1200 systems installed around the world used for numerous technologies. Prominent high volume manufacturing companies utilize NXQ's equipment for end products such as transceiver chip sets for cell phones and other wireless devices, medical and automotive sensors and advanced packaging applications. The company's products are also used extensively throughout the world at universities and research institutes and are recognized as one of the most versatile and flexible mask aligners in the marketplace. NXQ works closely with customers to innovate and develop new features and provide world class support that differentiate them from the competition. The company continues to gain market share with customers that require equipment suppliers who can meet their stringent needs for cost, performance and reliability. With the ability to process substrates in just about any shape and thickness, up to 300 mm, NXQ is well positioned to maintain double digit growth for the foreseeable future.

Booth: 37

NTK Technologies, Inc.

Santa Clara, CA USA
www.ntktech.com

NTK Technologies is a leader in IC Ceramic Packaging. With global service centers, NTK offers a wide range of packaging materials and package design services for Medical, Automotive, SiP/MCM, MEMS, Opto, RF, CMOS Image Sensors, Hi-Rel, Satellite, FCBGA, FCCSP, FPGA, CPU and MPU applications. Monolithic package designs for Medical and Mobile applications. Optimum package designs for 10G, 40G, and 100/400G. Large and small scale Ceramic STFs are manufactured for high-speed/high density probe-cards for semiconductor wafer test. Large and small scale ceramic substrates can be configured with narrow pitches and a wide range of pin count capabilities. NTK supports fast paced product cycle times with our advanced design and production flows featuring high precision processes for fast turn-around with the highest quality.

Booth: 23

Oneida Research Services Inc.

Englewood, CO USA
www.orslabs.com

Oneida Research Services, Inc. (ORS) provides analytical testing services to support the microelectronics, telecommunications, aerospace, automotive, medical, and defense industries. Our specialties include RGA testing, hermeticity testing, environmental and mechanical testing, materials and surface analysis, as well as DPA and component analysis. Companies come to ORS because of the wide range of specialized services that we offer. Our specialized laboratory testing is useful in product development, research, prototyping and quality control across a wide range of industries. ORS has been providing advanced testing services for over 40 years with a focus on research, development and quality control for our client's products.

Booth: 7

Onto Innovation

Wilmington, MA USA
www.ontoinnovation.com

Onto Innovation is a leader in process control, combining global scale with an expanded portfolio of leading-edge technologies that include: Unpatterned wafer quality; 3D metrology spanning chip features from nanometer scale transistors to large die interconnects; macro defect inspection of wafers and packages; metal interconnect composition; factory analytics; and lithography for advanced semiconductor packaging. Our breadth of offerings across the entire semiconductor value chain helps our customers solve their most difficult yield, device performance, quality, and reliability issues. Onto Innovation strives to optimize customers' critical path of progress by making them smarter, faster and more efficient. Headquartered in Wilmington, Massachusetts, Onto Innovation supports customers with a worldwide sales and service organization. Additional information can be found at www.ontoinnovation.com.

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Booth: 24

PacTech USA Packaging Technologies

Santa Clara, CA USA
www.pactech.com

Pac Tech - Packaging Technologies GmbH (group member of NAGASE & CO. Ltd.) is headquartered in Germany with wholly owned subsidiaries: PacTech USA Inc. in Silicon Valley, USA, and PacTech ASIA Sdn. Bhd. in Penang, Malaysia. PacTech is comprised of three business units: EQUIPMENT MANUFACTURING: Manual & Automatic ENIG & ENEPIG plating tools, Laser solder jetting equipment, Wafer-level solder ball transfer systems, Laser assisted flip-chip bonders. SUBCONTRACT SERVICES: Flip Chip and Wafer Level Package Bumping Services including ENIG or ENEPIG for UBM (solder bumping) or OPM (wirebond). Other services include Electroplating, Laser Solder Jetting, Wafer Level Solder Balling, Re-passivation, RDL, Backmetal, Wafer Thinning, Wafer Dicing, Tape & Reel, AOI, X-Ray, SEM, FIB. CHEMISTRY: Pre-Treatment and process chemistry for electroless plating.

Booth: 6

Palomar Technologies

Carlsbad, CA USA
www.palomartechnologies.com

Palomar Technologies is a leading supplier of automated microelectronic assembly machines and contract assembly services with specialization in precision die attach, wire bonding and vacuum reflow solutions. Palomar customers include RF, Optoelectronic and Defense market leaders. Headquartered in Carlsbad, CA, USA with established subsidiaries in Singapore and Germany, direct sales and service is provided in more than 25 countries around the world.

Booth: 52

PLASMA-THERM

St. Petersburg, FL USA
www.plasmatherm.com

Plasma-Therm is a global manufacturer of advanced plasma-processing equipment, providing etch, deposition, and plasma dicing technologies used in semiconductor packaging, solid-state lighting, power, data storage, renewable energy, MEMS, nanotechnology, photonics, and wireless communication markets. Plasma-Therm's VERSALINE platform is the workhorse for a variety of applications in specialty semiconductor markets. The platform's modular design allows flexible configuration of substrate handling and technologies that address the wide range of customer requirements. Plasma-Therm's Singulator® systems bring the precision and speed of plasma dicing to chip-packaging applications. Manufacturers, academic and governmental institutions depend on Plasma-Therm equipment, designed with "lab-to-fab" flexibility to meet the requirements of both R&D and volume production. Plasma-Therm's products have been adopted globally and have earned their reputation for value, reliability, and world-class support. Named the #1 Etch Equipment Supplier in 2019, Plasma-Therm has more than two decades of awards in the VLSIresearch Customer Satisfaction Survey, including the highest score ever earned by a semiconductor equipment company.

Booth: 29

Practical Components

Los Alamitos, CA USA
www.practicalcomponents.com

Practical Components is a leading international distributor of mechanical IC samples or "dummy" components (SMT and thru-hole) and evaluation PCB's and kits. We are the exclusive supplier of dummy components for Amkor Technology. We offer a variety of Advanced Test Wafers which are daisy-chained in a variety of pitches from 20um to 200um and are offered with Cu pillar with SnAg solder cap, SAC305 bumps, Ni with SnAg plate or with no bumps. We supply test vehicles for most of our components including the new SMTA Solder Paste Test Vehicle for Miniaturized Surface Mount Technology. Also, on display this year will be our new IPC/WHMA-A-620C-S space addendum training kit which meets or exceeds the requirements set in NASA-STD-8739.4 for wire harness assembly. Our Dummy Components save money if you need; Machine setup and evaluation; Assembly workflow evaluation; Cleanliness and Conformal Coating testing; Solder training, practice and certification; Soldering rework training; Prototyping, Demonstrations; Testing; CPK Studies, Process qualifications; validations;evaluations or Advanced Process Research.

Booth: 5

Quik-Pak

Escondido, CA USA
www.icproto.com

Quik-Pak, a division of Promex, provides IC packaging, assembly and wafer preparation services in our ISO 9001:2015, ITAR-registered facility. Our over-molded QFN/DFN packages and pre-molded air-cavity QFN packages offer a fast, convenient solution for prototype to full production needs; our thinning, dicing and sorting services for up to 300mm wafers are available standalone or as part of a turnkey project; and our same-day assembly services greatly reduce customers' time to market. Standard package sizes available that meet Jedec outlines, or we can design and fab custom substrates specific for your products.

Booth: 61

SemiDice, Inc

Los Alamitos, CA USA
www.semidice.com

SemiDice is the preferred global wafer and bare die component supplier to the microelectronic industry. SemiDice is the only global wafer processor with a High Reliability Division dedicated to providing bare die for military, aerospace, medical and robust industrial applications. With its headquarters in Los Alamitos CA and sales offices in the USA, United Kingdom and China, SemiDice is well-positioned to support customer requirements worldwide.

Booth: 25

SETNA Corporation

Chester, NH USA
www.set-na.com

High-accuracy Bonding Experience, Equipment, and Materials

SETNA is a Manufacturing and Marketing, Sales and Service Organization centered on our experience and know-how in high-accuracy bonding and the equipment, materials, competencies surrounding it. SET Bonders have been the world-standard for applications in which micron precision post bond accuracy is required, for more than twenty years the FC150 Series has been the tool of choice. The Ontos7 is our atmospheric plasma system designed for and dedicated exclusively to the semiconductor manufacturing and packaging industry. Our patented (and patent pending) equipment and processes provide a unique advantage to our customers to enable low-cost, high yield, high-speed, chip-to-chip interconnect bonds at room temperature with minimal force.

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Booth: 65

Sikama International, Inc.

Santa Barbara, CA USA
www.sikama.com

Sikama International Inc. designs and manufactures Solder Reflow and Curing Systems, Wafer Flux Coaters and Wafer Washers. With a solid 38 years in the industry, Sikama is recognized worldwide for our quality products and outstanding customer service. Sikama Machines feature a patented conduction plus convection heating technology and are used for Wafer Bumping, LED Die Reflow, BGA Re-balling, High Density Package Reflow, Lid Attach, Fluxless Gold Tin Reflow, Lead Frame Reflow, Epoxy Curing and many other applications. Please stop by Sikama Booth Number 65 to discuss your Reflow Soldering or Curing requirements.

Booth: 32

SPTS Technologies

Newport, UK
www.spts.com
Twitter: @SPTS_Tech

SPTS Technologies, a KLA company, designs, manufactures, sells, and supports advanced etch, PVD, CVD and MVD® wafer processing equipment and solutions for the global semiconductor and micro-device industries, with focus on the Advanced Packaging, MEMS, high speed RF device, power management and LED manufacturing.

SPTS has manufacturing facilities in Newport, Wales and Allentown, Pennsylvania, and operates across 19 countries in Europe, North America and Asia-Pacific. For more information please visit www.spts.com.

Find us on Twitter: @SPTS_Tech

Booth: 56

StratEdge Corporation

Santee, CA USA
www.stratedge.com

StratEdge, founded in 1992, designs, manufactures, and provides assembly services for a complete line of high frequency, power, and high reliability semiconductor packages. They operate from DC to 63+ GHz for the high-speed digital, mixed signal, broadband wireless, satellite, point-to-point/multipoint, VSAT, and test and measurement industries. StratEdge offers post-fired ceramic, low-cost molded ceramic, and ceramic QFN packages and specializes in packages for extremely demanding gallium arsenide (GaAs) and gallium nitride (GaN) devices. All packages are lead-free and most meet RoHS and WEEE standards. StratEdge Assembly Services, in our new ISO 9001:2015 facility near San Diego, CA, has a Class 1000 cleanroom and Class 100 work area with workstations for performing sensitive operations. It is fully equipped with the most modern assembly equipment, enabling StratEdge services to include high-speed fine wire wedge and ribbon bonding for deep access. The new component placement die attach system is the fastest and most reliable multiple die-type bonder on the market. It enables StratEdge Assembly Services to offer high-accuracy and peak repeatability and performance. StratEdge has a variety of lids and options for their attachment and offers post assembly services.

Booth: 59

SUSS MicroTec Inc.

Corona, CA USA
www.suss.com

The SUSS MicroTec Group is a leading supplier of equipment and process solutions for microstructuring applications with more than sixty years of engineering experience. Our portfolio covers a comprehensive range of products and solutions for backend lithography, wafer bonding and photomask processing, complemented by micro-optical components. ▪Photomask Equipment ▪Coater and Developer ▪Mask Aligner ▪Wafer Bonder ▪Micro-Optics ▪Remanufactured Equipment

Booth: 43

Technic

Cranston, RI USA
www.technic.com
Twitter: @Technicinc

Technic supplies some of the most advanced solutions for semiconductor fabrication and packaging in the industry including electroplating chemistry, photoresist strippers, cleaners (post etch residue removers), metal etchants, and high purity wet chemistry, as well as semiconductor manufacturing equipment. Technic's semiconductor electroplating chemistry, marketed under the name Elevate®, is well-respected globally for innovation and high quality. Elevate® processes offer high-performance electroplating for copper, nickel, tin and precious metals. Technic supplies photoresist strippers (for both liquid and dryfilm resist), metal etchants and cleaners (ie. post etch residue removers) for a variety of substrates used in wafer level surface preparation. Technic products provide a number of specific attributes that allow semiconductor manufacturers to remove many process limitations and take their technology to a new level. Our semiconductor fabrication and packaging chemistries are widely used in several advanced packaging platforms including FOWLP (Fan-Out Wafer Level Packaging), Fan-In WLP, Flip Chip and 2.5/3D. Technic's high-performance product development, with application specific characteristics and unparalleled analytical expertise, provides customers with the essential tools to meet the challenges of today's semiconductor manufacturing.

Booth: 21

TechSearch International, Inc.

Austin, Texas, USA
www.techsearchinc.com
Twitter: @Jan_TechSearch

TechSearch International, Inc. has a 30+ year history of market and technology trend analysis focused on semiconductor packaging, materials, and assembly. Research topics include WLP, FO-WLP and panel-level processing, Flip Chip, CSPs, BGAs, 3DICs, Si Interposers, System-in-Package (SiP) and Heterogeneous Integration, embedded components, ADAS and automotive electronics, and power devices. In conjunction with SavanSys Solutions, wire bond, flip chip, WLP, and 3D IC cost models are offered. TechSearch International professionals have an extensive network of more than 20,000 contacts in North America, Asia, and Europe and travel extensively, visiting major electronics manufacturing operations and research facilities worldwide.

Booth: 8

Teikoku Taping System Inc.

Phoenix, AZ USA
www.teikoku-taping.com/en/technology/

Our strengths revolve around "taping", that is, lamination and removal of protective tape and technologies associated with such processes, as well as technologies related to handling of wafers. We always keep up with the newest materials and technologies used in semiconductor fabrication to provide one-step-ahead turnkey solutions.

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Booth: 27

Towa

Minami-ku, Kyoto, Japan
www.towajapan.co.jp/en/

Towa is a Semiconductor company providing Transfer / Compression Molding and Package Singulation equipment for the Semiconductor Assembly Packaging Process. Towa revolutionized Transfer Molding by introducing the multi-plunger system and our Compression molding covers Strip / Wafer / Panel formats.

Booth: 10

Unisem

Santa Clara, CA USA
www.unisemgroup.com

Unisem is a global provider of semiconductor assembly and test services for many of the world's most successful electronics companies. Unisem offers an integrated suite of packaging and test services such as wafer bumping, wafer probing, wafer grinding, a wide range of leadframe and substrate IC packaging, wafer level CSP and RF, analog, digital and mixed-signal test services. Our turnkey services include design, assembly, test, failure analysis, and electrical and thermal characterization. With approximately 7,700 employees worldwide, Unisem has factory locations in Ipoh, Malaysia; Chengdu, People's Republic of China and Batam, Indonesia. The company is headquartered in Kuala Lumpur, Malaysia.

Booth: 49

XPERI / Invensas

San Jose, CA USA
www.invensas.com

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Booth: 60

XYZTEC

Panningen, The Netherlands
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XYZTEC is the global technology leader in bond testing. The Condor Sigma is the most advanced bond tester available to support technical end-users working in electronics hardware assembly & test applications that require either destructive or non-destructive bond testing. The Rotating Measurement Unit (RMU) enables continuous operation with up to six different test types on one machine at forces up to 200kgf. XYZTEC also offers novel solutions for battery & high-force applications.

Booth: 58

Yole Développement

Villeurbanne, France
www.yole.fr
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Yole Développement provides market research, technology analysis, strategy consulting, targeted media, and financial advisory services. With a strong focus on emerging applications using silicon and/or micro manufacturing since 1998, Yole Développement has expanded to include more than 80 collaborators worldwide covering Photonics – Lighting – Imaging – Sensing & Actuating – Display – RF Devices & Technologies – Compound Semiconductors & Emerging Materials – Power Electronics – Batteries & Energy Management – Semiconductor Packaging and Substrates – Semiconductor Manufacturing – Memory – Computing and Software. The market research, technology and strategy consulting company Yole Développement, along with its partners System Plus Consulting, PISEO and KnowMade – all part of the Yole Group of Companies-, support industrial companies, investors and R&D organizations worldwide to follow technology trends to grow their business and help them understand the 6 specific markets.

Booth: 35

Zuken, Inc.

San Jose, CA USA
www.zuken.com/us/
Twitter: @ZukenAmericas

Zuken is a global provider of leading-edge software and consulting services for system-level electrical and electronic design and manufacturing. Founded in 1976, Zuken has the longest track record of technological innovation and financial stability in the electronic design automation (EDA) software industry for advanced packaging, printed circuit board design, and multi-domain co-design. The company's extensive experience, technological expertise and agility, combine to create world-class software solutions. Zuken's transparent working practices and integrity in all aspects of business produce long-lasting and successful customer partnerships that make Zuken a reliable long-term business partner. Zuken is focused on being a long-term innovation and growth partner. The security of choosing Zuken is further reinforced by the company's people— the foundation of Zuken's success. Coming from a wide range of industry sectors, specializing in many different disciplines and advanced technologies, Zuken's people relate to and understand each company's unique requirements.

Booth: 26

Zymet, Inc.

East Hanover, NJ USA
www.zymet.com

Adhesives and encapsulants for electronics and optoelectronics assembly. Products include reworkable and non-reworkable underfill encapsulants, edgefill adhesives, and edgebond adhesives for high reliability board level assembly. Products also include electrically conductive and thermally conductive adhesives, ultralow stress adhesives, ACP's and NCP's, and UV curable encapsulants.

MONDAY, MARCH 2, 2020				**Professional Development Courses (PDCs)**
7:00 am – 7:00 pm	*REGISTRATION*			
10:00 am – 12:00 pm *2-HOUR FORMAT*	***MORNING*** Professional Development Courses (PDCs) – **10:00am-12:00pm**			
	PDC1: Introduction to Fan Out Packaging *CANCELLED*	PDC2: System-in-Package (SiP) - System Solutions Through Miniaturization Course Leaders: Mark Gerber, ASE Group	PDC3: Basics of Conventional and Advanced Chip Packaging Course Leader: Syed Sajid Ahmad, CrossFire Tech	
12:00 pm – 1:00 pm	***LUNCH*** *(boxed lunches can be picked up in the foyer from 12-12:30pm)* *Only provided for those attendees registered for BOTH Morning and Afternoon PDCs*			
1:00 pm – 3:00 pm *2-HOUR FORMAT*	***EARLY AFTERNOON*** Professional Development Courses (PDCs) – **1:00pm-3:00pm**			
	PDC4: Development of Advanced Fan Out Technologies Course Leader: John Hunt, ASE Group	PDC5: 3D Package Assembly and Technology for Mobile Devices Course Leader: Tom Dory, Fujifilm Electronics Materials	PDC6: Gold-Aluminum Intermetallics Course Leader: Syed Sajid Ahmad, CrossFire Tech	PDC7: Fundamentals of 5G Course Leader: Ivan Ndip, Fraunhofer IZM
3:00 pm – 3:30 pm	*COFFEE BREAK IN FOYER*			
3:30 pm – 5:30 pm *2-HOUR FORMAT*	***LATE AFTERNOON*** Professional Development Courses (PDCs) – **3:30pm-5:30pm**			
	PDC8: Advances in Fan-Out Wafer Level Packaging (FOWLP) Course Leader: Beth Keser, Intel Corporation	PDC9: The Evolution of Flip Chip Package Technology Course Leader: Mark Gerber, ASE Group	PDC10: Polymers in Wafer Level Packaging Course Leader: Jeffrey Gotro, InnoCentrix, LLC	PDC11: Advanced Assembly Processes of Wafer Level Fan Out Packaging *CANCELLED*
5:30 pm – 7:00 pm	WELCOME RECEPTION (*All registered Conference attendees are invited to attend*)			

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TUESDAY, MARCH 3, 2020	Morning Technical Sessions
7:00am-7:00pm	*Registration*
7:00am-8:00am	*Continental Breakfast Sponsored by:* DUPONT, NAMICS, Mentor A Siemens Business, cadence, EMD Performance Materials
8:00am-8:20am	OPENING COMMENTS General Chair: Rama Puligadda, Brewer Science *Plenary/Keynote Sessions Sponsored by:* (ROOM 107-108) SPTS A KLA Company
8:20am-9:05am	KEYNOTE 1: *HETEROGENEOUS INTEGRATION TECHNOLOGIES FOR MOORE'S LAW 2.0 AND BEYOND* *This speech presents a vision and long-term semiconductor technology migration path to achieve two critical goals- extension of Moore's Law and to enable energy-efficient AI compute. Holistic WLSI, a disruptive wafer-level heterogeneous integration technology platform as an example, can realize micro-system scaling in wafer form at conventional front-end stage as well as back-end stage to achieve the above-stated goals.* *Douglas Yu, Vice President R&D, TSMC* *Dr. Yu is a Vice President of TSMC R&D, responsible for the development of advanced Integrated Interconnect & Packaging technologies. He has been in charge of on-chip interconnects (Cu/Low-K and Cu/ELK), and wafer-level system integration (WLSI including CoWoS®, InFO and SoICTM, etc.) technology developments. These are the first technologies introduced to set new standards and start a new trend for semiconductor industry.* *Doug worked with AT&T Bell Labs previously. He received his Ph.D. in Materials Engineering from Georgia Institute of Technology. Dr. Yu is an IEEE Fellow in recognition of his leadership in IC interconnect technology development. He was awarded President Science Prize, among the most prestigious Taiwan science award. Doug has been granted 1000+ US patents. He has over 150 technical publications with numerous plenary, keynote and invited speeches in leading international conferences, plus several semiconductor book chapters.*
9:10am-9:55am	KEYNOTE 2: *RF FRONT END PACKAGING CHALLENGES IN 5G* *Mobile Technology in general and cell phones in particular have been a driving factor for electronic packaging innovations since the beginning and at the same time packaging innovations have been an enabler for more user-friendly form factors and / or increased functionality. The introduction and worldwide ramp of 5G marks a new turning point in this relationship as the capabilities of handsets are significantly improving and requirements for RF packaging are getting more demanding. The RF front end (RFFE) is a major contributor to these enhanced capabilities as it forms the link between the modem and the network.* *5G presents additional challenges to the RF front end design when compared to the 3G / 4G transition. These challenges come from various aspects of 5G such as the increased bandwidth of the new sub 6 GHz frequency bands, the option to operate 4G and 5G in the sub 6 GHz frequency range at the same time, the introduction of mm wave frequencies to the RF front end and the generally stricter requirements on signal integrity.* *While technical solutions for most of these challenges already exist in some form it becomes a challenge of its own to provide them in a package that is compatible with today's mobile phone designs.* *Dr. Christian Hoffmann, Principal Engineer, Qualcomm Germany RFFE GmbH* *Christian Hoffmann is a member of the New Technology Business Development organization of the RFFE business unit and is responsible for technology pathfinding in the area of RF packaging. He joined Siemens Matsushita Components in Deutschlandsberg / Austria in 1998 as development engineer for RF ceramic materials and base station products before becoming head of technology development for the newly established LTCC technology in 2001. After 2006 he was responsible for all ceramic material research & development in Deutschlandsberg and when TDK acquired EPCOS in 2008 Christian Hoffmann became the 1st EPCOS engineer to work at the TDK R&D headquarter in Ichikawa / Japan. Returning to Germany in 2014 he started at the CTO Office of the SAW business group which after the acquisition by Qualcomm became the New Technology Business Development department of the RFFE BU. Christian Hoffmann is a member of the American Ceramic Society and IMAPS and helped to bring both societies together for a new conference series which would become CICMT. He served as technical co chair for CICMT and as general co chair of the 1st CICMT event outside of the US 2008 in Munich / Germany. Christian Hoffmann has a diploma in Physics and a doctor degree in Electrical Engineering from the University of Aachen / Germany.*
9:55am-10:00am	CONFERENCE LEADERSHIP RECOGNITION General Chair: Rama Puligadda, Brewer Science
10:00am-6:30pm	EXHIBITION OPEN (WASAJA BALLROOM)
10:00am-10:30am	*Break in the Exhibit Hall Sponsored by:* PacTech member of nagase group

	3D INTEGRATION Track ROOM 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track ROOM 104-106	ADVANCED PACKAGING & EMERGING MATERIALS for AUTOMOTIVE, 5G & NEXT GEN APPLICATIONS Track ROOM 102-103
TUESDAY MORNING SESSIONS:	T-AM1: APPLICATION & DESIGN Chairs: Dongshun Bai, Brewer Science; Vik Chaudhry, Amkor Technology	T-AM2: CHALLENGES IN FAN-OUT WAFER LEVEL PACKAGING Chairs: Beth Keser, Intel Corporation; Nokibul Islam, JCET Group	T-AM3: AUTOMOTIVE PACKAGING TRENDS Chair: Prasad Dhond, Amkor Technology
10:30am-11:00am	032 *This is Not Your Father's Semiconductor Packaging…An EDA Perspective* John Park, Cadence Design Systems	042 *Design Process & Methodology for Achieving High-Volume Production Quality for HDFO Packaging* Ruben Fuentes, Amkor Technology (Keith Felton, Mentor, a Siemens Business)	064 *Automotive Packaging Trends - Challenges and Solutions* Eungsan Cho, Infineon Technologies Americas Corp. (Thorsten Meyer)
11:00am-11:30am	012 *Silicon Capacitor Highly Integrated in Medical Systems Thanks to the Embedded Technology* Catherine Bunel, MURATA (Mickael Pommier)	048 *RF Analysis of Fan-Out Wafer Level Packaging Concepts with Integrated Antennas for 5G Applications* Ivan Ndip, Fraunhofer IZM (Marco Rossi, Tanja Braun, Thi Huyen Le, Abhijeet Kanitkar, Friedrich Müller, Marcel Wieland, Christian Goetze, Saquib Bin Halim, Jean Trewhella, Klaus Dieter Lang)	041 *Achieving Success in Automotive Leadframe Packages* John Nickelsen, Amkor Technology
11:30am-12:00pm	066 *Samsung Foundry's 3D PKG Solution based on Cadence Design Flow* Max Min, Samsung Foundry US (SungWook Moon)	060 *Fan Out Wafer Level Package with Enhanced Product Reliability and Advanced Node Silicon Chip Package Integration* Gaurav Sharma, NXP Semiconductors (Nishant Lakhera, Craig Beddingfield, Mollie Benson, Andrew Mawer)	062 *Design and Process Considerations for Using Flip-chip Packaging Technology for the Automotive Market* Vinayak Pandey, JCET Group (Nokibul Islam)
12:00pm-12:30pm	058 *Thermal Management Implications for Heterogeneous Integrated Packaging* Cameron Nelson, Amkor Technology	006 *Reliability Simulation with the Finite Element Analysis (FEA) of Redistribution Layer in Fan-out Wafer Level Packaging (FOWLP)* Yuji Okada, Asahi Kasei Corporation (Akira Fujii, Kenta Ono, Yoshiharu Kariya)	052 *Copper Wire Ready for Automotive AEC Requirements?* William Crockett, Tanaka Kikinzoku International (America)
12:30pm-2:00pm	*Lunch Break in the Exhibit Hall Sponsored by:* 		

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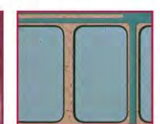
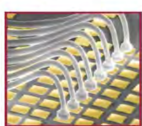

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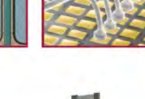

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TUESDAY, MARCH 3, 2020			**Afternoon Technical Sessions**
	3D INTEGRATION Track ROOM 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track ROOM 104-106	ADVANCED PACKAGING & EMERGING MATERIALS for AUTOMOTIVE, 5G & NEXT GEN APPLICATIONS Track ROOM 102-103
TUESDAY AFTERNOON SESSIONS:	T-PM1: TECHNOLOGY - ORGANIC & SILICON BASED 3D Chairs: Suresh Jayaraman, Amkor Technology; Stevan Hunter, ON Semiconductor; Marco Del Sarto, STMicroelectronics	T-PM2: ADVANCES IN PROCESS, MATERIALS, AND EQUIPMENT FOR FAN-OUT WAFER LEVEL PACKAGING Chairs: Curtis Zwenger, Amkor Technology; Farhad Kiaei, HD MicroSystems	T-PM3: AUTOMOTIVE and 5G SIPs Chairs: Tu-Anh Tran, NXP Semiconductors; Bora Baloglu, Amkor Technology
2:00pm-2:30pm	016 *An Embedded Planar-Foil Capacitor Material FPGA Interposer Aimed at Improving System Performance and Reduce Board Size for Space Based Electronics* Don Hunter, Jet Propulsion Laboratory (Gary Bolotin, Malcolm Lias, Ben Cheng)	043 *Enabling Fine Line RDL and High Aspect Ratios for Cu Pillars for Heterogeneous Integration* Fabian Benthaus, Suss MicroTec (Yajun Gu, Habib Hichri, Markus Arendt)	036 *The New Technology Solutions for Advanced SiP Devices* YongJai Seo, Amkor Technology
2:30pm-3:00pm	021 *PCB embedding of Magnetic Material for Inductor-based Applications* Gerald Weis, AT & S Austria Technologie & Systemtechnik Aktiengesellschaft	013 *Improving WID and WIW Non-Uniformity in ECD Applications* Charles Sharbono, Applied Materials	047 *Application of Vertically Aligned CNT Sheets to Die Attachment for Future Power Semiconductor Devices* Daiyu Kondo, Fujitsu Laboratories Ltd. (Shinichi Hirose, Koichi Suzuki, Masaaki Norimatsu, Yu Oyama, Shintaro Sato)
3:00pm-3:30pm	056 *Adaptive High Density RDL Technologies for Panel Level Packaging* Lars Boettcher, Fraunhofer IZM (S. Kosmider, F. Schein , R. Kahle, A. Ostmann)	001 *Embedded Trace and RDL Copper Plating Process for Panel Level Packaging Applications* Kesheng Feng, MacDermid Alpha Electronics Solutions (Saminda Dharmarathna, William Bowerman, Jim Watkowski, Leslie Kim, Johnny Lee)	082 *Enhancing the Punch MLF®/QFN Package for Improved Robustness in Automotive Applications* Marc Mangrum, Amkor Technology
3:30pm-4:00pm	*Break in the Exhibit Hall Sponsored by:* Quik-Pak™ Microelectronic Packaging & Assembly Solutions		
4:00pm-4:30pm	007 *Through Silicon Via Undercut Profile Optimisation for 3D Packaging Applications* Paul Gray, SPTS Technologies (Janet Hopkins, Huma Ashraf, Lijie Li)	054 *Multipurpose Use of Laser-Sensitive Materials for Temporary Bonding and Debonding Applications in Wafer-Level Packaging* Luke Prenger, Brewer Science (Xiao Liu, Lisa Kirchner, Xavier Martinez, Samantha Oelklaus, Rama Puligadda)	002 *Advanced Double Side SiP with Thermal Enhance Solutions for 5G Mobile Application* Mike Tsai, SPIL (Ryan Chiu, Eric He, J. Y. Chen, Frank Chu, Jensen Tsai, Yu-Po Wang, Shunyu Jian, Simon Chen)
4:30pm-5:00pm	046 *Thin Quad Die Package (QDP) Development* Shaun Bowers, Amkor Technology, Inc.	053 *Latest Technology of Epoxy Molding Compound (EMC) for FO-WLP* Takeshi Mori, Sumitomo Bakelite Co.,Ltd.	030 *A New Level of Connectivity- 5G Package Considerations* Mark Gerber, ASE US Inc.
5:00pm-5:30pm	070 *PCB Embedding Technology for 5G mmWave Applications* Stefan Kosmider, Fraunhofer IZM (Kavin Murugesan, Te Huyen Le, Uwe Maaß, Marco Rossi, Lars Boettcher)	057 *Die Crack Prevention and Detection in Advanced Packaging* Woo Young Han, ONTO Innovation	050 *3D Integrated Antennas for Millimeter-Wave and Terahertz Wireless Communication and Radar Sensing* Ivan Ndip, Fraunhofer IZM (Thi Huyen Le, Klaus-Dieter Lang)
5:30pm-6:30pm	*Break in the Exhibit Hall Sponsored by:* TECHNIC INC XPERI Semiconductor Technologies | invensas		
6:30pm-8:00pm	EVENING KEYNOTE & PANEL DISCUSSION (*ROOM 107-108)* *DETAILS ON THE FOLLOWING PAGE*		

6:30pm-8:00pm	**EVENING KEYNOTE & PANEL DISCUSSION** (*ROOM 107-108)* *Panel Session & Refreshments Sponsored by:* **EVENING PANEL DISCUSSION:** ***High Performance Computing: Are Chiplets the Answer?*** **Moderators:** Jan Vardaman, TechSearch International; Beth Keser, Intel Corporation **Panelists:** Robert Patti, NHanced Semiconductors, Inc.; Douglas Yu, TSMC Max Min, Samsung; Microsoft, Intel, and zGlue (Others TBD) *No longer can the industry count on monolithic integration to achieve the economic gains of the previous era. New packaging solutions are being adopted to achieve the economic advantages that were previously met with silicon scaling. The role of heterogeneous integration, especially chiplets, is pivotal in this new era. TSMC indicates that the use of chiplets will be one of the most important developments for the next 10 to 20 years. A chiplet is a functional circuit block and includes reusable IP blocks. A chiplet can be created by partitioning a die into functions and is typically attached to a silicon interposer or organic substrate today, but new options are emerging such as advanced fan-out, RDL interposer, embedded bridges, and 3D packaging. This panel discussion provides insight into some of the applications driving the use of chiplets and explores challenges in bringing this into HVM.*

WEDNESDAY, MARCH 4, 2020 GBC Plenary Session

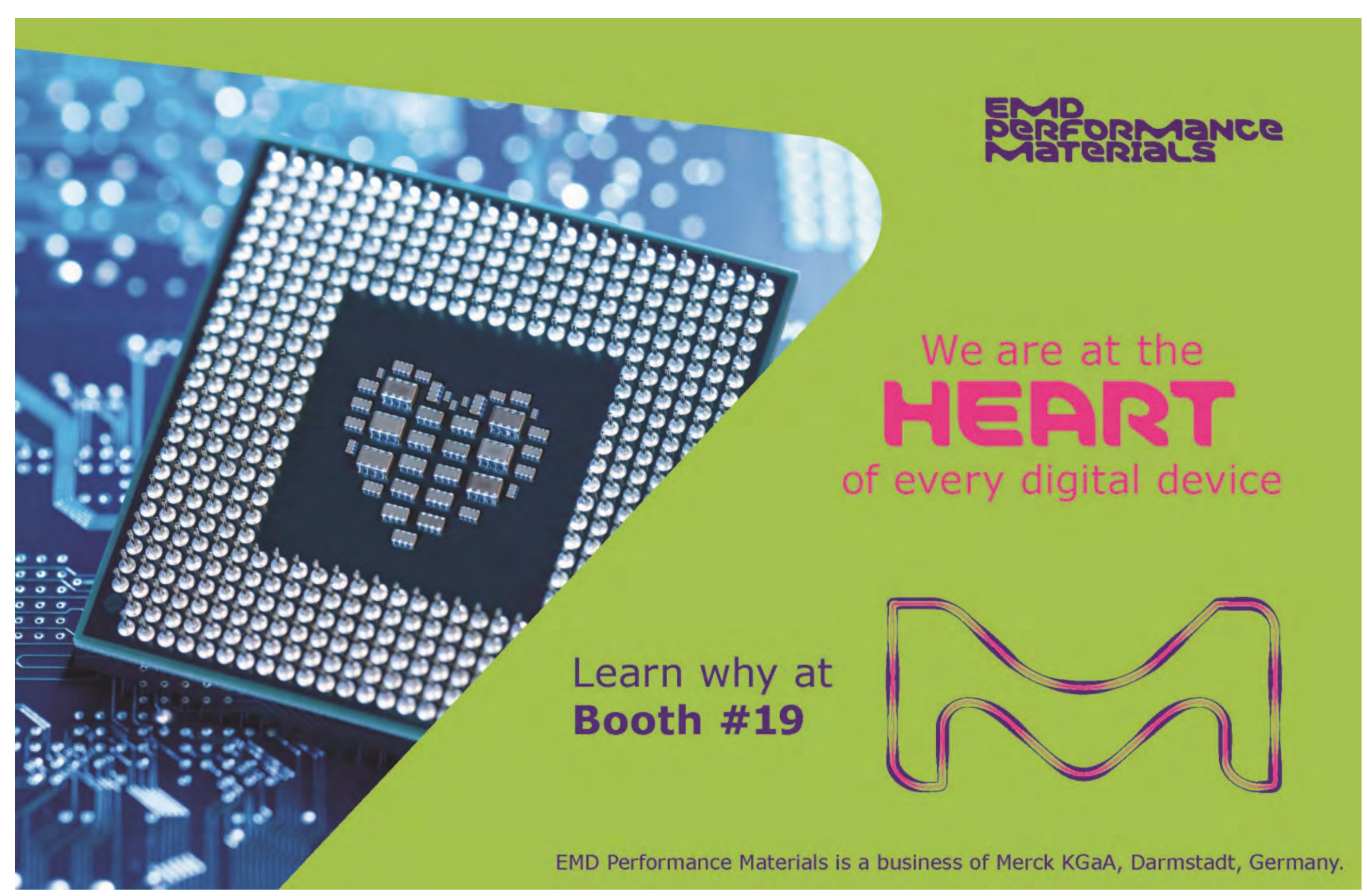
Welcome to the Global Business Council (GBC) Plenary Session on

ELECTRONICS INDUSTRY TRANSITION

OPENING COMMENTS:
GBC Chairs: Lee Smith, Consultant; Rich Rice, ASE Group; Thomas Goodman, Izinus

Time	Session
7:00am-6:00pm	*Registration*
7:00am-8:00am	*Continental Breakfast Sponsored by:* DUPONT, NAMICS, Mentor A Siemens Business, cadence, EMD Performance Materials
8:00am-8:15am	*GBC OPENING COMMENTS* GBC Chairs: Lee Smith, Consultant; Rich Rice, ASE Group; Thomas Goodman, Izinus *Plenary/Keynote Sessions Sponsored by:* (*ROOM 107-108*) SPTS A KLA Company
8:15am-8:45am	*HETEROGENEOUS INTEGRATION, DIELETS AND CHIPLETS – WHY THE HYPE?* Subramanian "Subu" S. Iyer, Distinguished Professor and Charles P. Reames Endowed Chair, UCLA *Looking at the news media and technical literature, one would think that the world has just discovered heterogeneous integration. In reality packaging has always been about heterogeneous integration. What is new is the scale of this integration in terms of connection pitches and the newer technologies that can presumably take this to the next level, including the fact that chiplets/dielets will be an increasingly important part of the ecosystem. This talk will explore these aspects and the implications on the eco-system and supply-chain in the area of high-performance computing, especially machine learning and AI, consumer electronics and medical electronics.*
8:45am-9:15am	*INTEGRATION TECHNOLOGIES TRANSFORMING THE WORLD* Yin Chang, SVP Sales & Marketing, ASE Group *The electronics industry is transforming our world, significantly driven by semiconductor innovation that is enabling life-changing applications from health to transportation, from virtual reality to AI. Advances in silicon integration technologies are proving truly revolutionary, where multiple die from multiple sources of varying functionality, are being combined to achieve unprecedented performance and operating characteristics. The packaging industry is at the forefront for the enablement of this integration. With a comprehensive tool box leveraging innovative technologies such as 2.5D & 3D die interconnection, high density fan-out, embedded devices, conformal and compartmental shielding, integrated antenna, and more, System-in-Package (SiP) portfolios are constantly being refined and enhanced to support growing demand for next generations of system integration. During his talk, Yin Chang will describe the expanding application landscape, discuss integration technology innovation, and explore how SiP technologies are delivering on their promise of miniaturization, power efficiency, and highest performance yet.*
9:15am-9:45am	*INTERCONNECT TRANSITIONS AND THE CHALLENGE AHEAD* E. Jan Vardaman, President and Founder, TechSearch International, Inc. *Wire bond still accounts for the majority of semiconductor package interconnect, but the strongest growth is in advanced packages such as flip chip and wafer level packages. On the horizon is hybrid bonding or direct bond interconnect. This presentation discusses interconnect transitions, including developments in existing interconnect methods such as wire bonding, tape automated bonding (TAB), and copper clip bonding. The need for the infrastructure development to support a major change in interconnect technology is discussed. The drivers and challenges for the new era in hybrid bonding are explored.*
9:45am-10:45am	*Break in the Exhibit Hall Sponsored by:* (*Wasaja Ballroom*) METALOR®

10:45am- 11:15am	*ADVANCED PACKAGING LEAD SEMICONDUCTOR TRANSITION INTO THE NEXT DECADE* **Vaibhav Trivedi, Sr. Technology Market Analyst, Yole Development** *Over last decade, advanced packaging such as fan-out wafer or panel level, side molded WLCSP, and SiP have changed the landscape of the semiconductor supply chain driven by mobile applications. This presentation will explore advancements in advanced packaging technologies in terms of scaling, heterogenous integration, and advanced packaging process development over last ten years and provide insight on how this will shape the next decade.* *A deep dive into the trends and advancements for fan-out wafer and panel level packaging will be explored as these technologies are impacting the overall packaging supply chain including: IDM, Foundry, OSAT and substrate supply. Fan-out packaging will be addressed as a vehicle and enabler supporting industry transition with its various configurations from package/process standpoint.*
11:15am- 11:45am	*RECOVERY: WHEN DID IT START…WHAT DROVE IT…HOW LONG WILL IT LAST* **Andrea Lati, Vice President, Market Research, VLSI Research** *2019 was a tough year for the industry with both IC and Equipment sales falling by double digits. Unlike the previous cycles, the equipment market fared better than semiconductors in 2019, powering out of downturn territory in the second half of the year. So what will 2020 bring for the industry? Will the equipment market continue to lead semiconductors and maintain the momentum?* *Some of the questions to be addressed in the presentation include:* *What is the growth range that can be expected?* *How will this growth be achieved?* *What are the key drivers and pivot points?* *How are current trends and issues likely to unfold in the coming year?* *Where will the best markets and opportunities be?*
11:45am- 12:00pm	*GBC CLOSING REMARKS*
12:00pm- 1:30pm	***Lunch Break in the Exhibit Hall Sponsored by:*** Amkor Technology® JCET SemiDice Wafer & Die Products



WEDNESDAY, MARCH 4, 2020 — Afternoon Technical Sessions

	3D INTEGRATION Track ROOM 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track ROOM 104-106	ADVANCED PACKAGING & EMERGING MATERIALS for AUTOMOTIVE, 5G & NEXT GEN APPLICATIONS Track ROOM 102-103
WEDNESDAY AFTERNOON SESSIONS:	W-PM1: TECHNOLOGY – 3D SILICON & GLASS Chairs: Rafiqul Islam, Cactus Materials; Lars Böttcher, Fraunhofer IZM	W-PM2: PACKAGING ADVANCES IN HIGH PERFORMANCE COMPUTE Chairs: Scott Hayes, NXP; Jae Kyu Cho, Global Foundries	W-PM3: NEXT GEN APPLICATION SOLUTIONS Chair: Linda Bal, TechSearch International; Jon Aday, Illumina
1:30pm-2:00pm	059 *Heterogeneous Packaging, Chiplets and the Quest for Higher Performance* Mike Kelly, Amkor Technology (Dave Hiner, Curtis Zwenger, George Scott, Ron Huemoeller)	014 *Fluxless Thermocompression Flip Chip Bonding Via In-Situ Oxide Reduction Bonding* Bob Chylak, Kulicke and Soffa Industries (Tom Colosimo, Adeel Bajwa, Horst Clauberg)	037 *Chip-to-Chip Integration for High Bandwidth Memory Processor Interface* Andy Heinig, Fraunhofer IIS/EAS (Fabian Hopsch)
2:00pm-2:30pm	076 *In-process Warpage Prediction and Optimization for Heterogeneously Integrated Packages Using a Novel Thermo-mechanical Modeling Scheme* Priyal Shah, Advanced Micro Devices, Inc. (Milind Bhagavat)	010 *10 micron Pitch Wiring and Bump on Substrate Formed by Imprinting Technology to Apply Low Temperature Flip Chip Bonding* Hiroshi Komatsu, CONNECTEC JAPAN Corporation (Nozomi Shimoishizaka, CONNECTEC JAPAN Corporation; Toshihiro Yamada, Industrial Research Institute of Niigata Prefecture)	011 *Low Cost EMI Shielding Using Silver Particles and CNTs* Byounggug Min, Samsung Electronics (Min woo Song, Jongkak Jang, SangHo An)
2:30pm-3:00pm	071 *3D Packaging. MEMS and Sensor Point of View* Marco Del Sarto, STMicroelectronics	028 *Applications of Novel High-speed In-line Automatic X-ray Inspection in High-volume Manufacturing* Frank Chen, SVXR, Inc.	038 *Coating Adhesion Testing for Improved RF* Thomas Monaghan, Knowles Corp
3:00pm-4:00pm	*Break in the Exhibit Hall Sponsored by:* (*Wasaja Ballroom*) SPECTRUM SEMICONDUCTOR MATERIALS, INC.		
4:00pm-4:30pm	069 *Glass Interposers Using Cu-plated Through Glass Vias (TGVs)* Charles Woychik, i3 Microsystems, Inc. (Justin Borski, Robert Nead)	004 *Solution for Accelerator Wall of HPC with HBM Integrated Packages* JinWei You, Siliconware Precision Industries Co. Ltd (Yu-Po Wang, Cheng Kai Chang, Teny Shih, Nicholas Kao)	008 *Prototyping IoT Modules Assembled by Additive Manufacturing* Yoko Fujita, Zuken Inc.
4:30pm-5:00pm	074 *Leading Edge Glass Interposer for High frequency application* Satoru Kuramochi, Dai Nippon Printing co Ltd (Masaya Tanaka)	039 *Decision System In Package in IoT/5G Application* Tuan Hoang, Zuken Inc.	019 *Advancements and Integration of Thin Glass Solutions* Aric Shorey, Mosaic Microsystems (Shelby Nelson, David Levy, Paul Ballentine)
5:00pm-5:30pm	079 *Cu Interconnect Scaling with Hybrid Bonding for 2.5 and 3D Integration* Laura Mirkarimi, Xperi (Thomas Workman, Gill Fountain, Guilian Gao, Jeremy Theil, Gabe Guevara, Bongsub Lee, Dominik Suwito, Pawel Mrozek)	045 *Backside Metallization for Low Cost High Thermal Package* Nokibul Islam, JCET Group (Chris Scanlan, WQ Jin, SY Chai)	023 *Micro-Features in Glass using Laser Induced Deep Etching for Device Packaging* Jean-Pol Delrue, LPKF Laser & Electronics (Rafael Santos, Norbert Ambrosius, Roman Ostholt, Stephan Schmidt)

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POSTER SESSION & HAPPY HOUR

Outside on Patio Overlooking Desert: 5:30 pm - 6:30 pm

(Poster Presenter Setup - 4:00 pm - 5:25 pm)

Poster Session & Happy Hour (5:30pm-6:30pm) Sponsored by:

005
An Instrumented Getter for Hermetically Sealed Packages
Robert Dean, Auburn University (Michael Previti)

018
Novel Low Temperature Curable Photo-Patternable Low Dk/Df for Wafer Level Packaging (WLP)
Katie Han, Kayaku Advanced Materials/Nippon Kayaku (Yasumas Akatsuka, Jenna Cordero, Shinya Inagaki, Daniel Nawrocki)

024
Dual-cure Sealing of Assemblies for Automotive Manufacturing
John Moore Daetec LLC (R Gorski, N Kreiner, C Padfield, H Rehman, A Riekenbrauck, C Davis, T "TJ" Fagòt, A Gray)

031
Damping Materials for Shock Performance of Micromachined Vibration Isolators
Brent Bottenfield, Auburn University (Artie Bond, Mike Kranz, Brian English, Robert Dean, Mark Adams)

033
Assembly of Intradermic, Micro, Silicon Needle Using Standard Die Bonding Equipment
Jonathan Abdilla, BESI Austria GmbH (Zlatko Hajdarevic, Hannes Klingler, Lars Zondervan)

040
Thermal Cycling of Aerosol Jet(R) Printed Silver Interconnects
Kurt Christenson, Optomec (Patrick Welch, Shaun Bowers, Knowlton Olmstead)

063
New Technology Paths for Next Generation Packaging Using Advanced Innovative Laser Assisted 3.5D and SB2-WB Assembly Processes
Thomas Oppert, PacTech - Packaging Technologies GmbH (Matthias Fettke, Andrej Kolbasow, Thorsten Teutsch)

065
Computational Simulation of the Molecular Structure and Properties of MPS and SH110 in TSVs Copper Filling
Yuping Le, Central South University (Fuliang Wang)

067
Thermal Interface Material Dispense in Power Module and 5G Device Package Applications
Hanzhuang Liang, Nordson Asymtek

072
Early Detection of Photoresist Contamination in Plating Baths - Inline Process Control Methodology
I. Popova, Ancosys Inc. (N. Schroeder, R. Dickman, R. Suter, J. Stahl)

073
Trends in Fan-Out Wafer Level Processing: 600mm Panel Level for 6-Sided Die Protection M-Series
Jacinta Aman Lim, nepes corporation (Jay Kim, YM Park, Brett Dunlap)

075
Contamination Troubleshooting for Microelectronics Packaging
Victor K.F. Chia, Air Liquide Electronics - Balazs NanoAnalysis

077
Low Dielectric Loss Polyimide B-stage Sheet
Masao Tomikawa, Toray Industries Inc. (Akira Shimada, Hitoshi Araki)

078
Acceleration Factors and Life Predictions
Chris South, Ansys - DfR Solutions

080
Carbon Nanofiber MIM Capacitors with Ultra-high Capacitance Densities, Low ESR and Large Operating Temperature Range
Vincent Desmaris, Smoltek AB (Sascha Krause, Rickard Andersson, Maria Bylund, Amin Saleem, Victor Marknas, Shafiq Kabir)

081
Dynamic Maskless Aligner lithography: Flexibility for Packaging Applications
Philip Paul, Heidelberg Instruments Mikrotechnik GmbH

NEW
Manufacturing Technology Solution as Heterogeneous Integration for Future In-memory Computing
Yasuhiro Morikawa, ULVAC

ALSO PRESENTED IN SESSION TH-AM3
026
Online Monitoring of Panel Level Packaging Process Solutions
Michael Pavlov, ECI Technology (Karsten Andrae, William Finck, Jingjing Wang, Eugene Shalyt, Paul Okagbare, Vishal Parekh, Michael MacEwan)

2020 3D InCites "Bonus Happy Hour" & Awards Ceremony

6:30pm-7:30pm

Immediately Following the Poster Session - Outside On Patio Overlooking Desert (Weather Permitting)

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THURSDAY, MARCH 5, 2020 — Morning Technical Sessions

Time	Session
7:00am-11:30am	*Registration*
7:00am-8:00am	*Continental Breakfast Sponsored by:*
7:55am-8:00am	*OPENING COMMENTS* General Chairs: Rama Puligadda, Brewer Science; Eric Huenger, DuPont Electronic & Imaging *Plenary/Keynote Sessions Sponsored by:* (*ROOM 107-108*) SPTS A KLA Company
8:00am-8:45am	KEYNOTE 3: ***INTEGRATED WAFER LEVEL PACKAGING TECHNOLOGIES FOR HIGH-PERFORMANCE COMPUTING SYSTEMS: CHALLENGES AND OPPORTUNITIES*** *Higher computing power and memory bandwidth are the major requirements of AI and 5G for GPU, accelerators and network devices. These demands lead to the adoption of the advanced packaging technologies to increase bandwidth density and to improve electrical performance with shorter interconnection length. For consumer application, panel level fan-out technologies are being used for consumer and mobile devices due to smaller form factors and higher electrical/thermal performances. Also, 3D TSV technologies provide high bandwidth density within a limited footprint. For network applications, 2.5D and 3D technologies are employed for cloud and artificial intelligence (AI). High-performance chip size continues to increase up to one reticle size and the cost of the leading-edge silicon node is recently soaring. So various chiplet packaging solutions, such as 2D, 2.5D and 3D are necessary to develop with the fine pitch bonding process and fine pitch interconnection evolutions. In this presentation, the above mentioned integrated wafer level packaging solutions are to be introduced and discussed in terms of challenges and opportunities for emerging high-end computing platforms. Furthermore, a high-performance 3D SiP system is introduced for signal/power efficiency and the extension of the fanout package for network/server application.* *Max Min, Samsung & Seung Wook Yoon, Corporate VP, Samsung Electronics* *Dr. YOON is currently working as Corporate VP/Head of Team of Package Technology Planning, Test & System Package, Samsung Electronics. Prior to joining Samsung, He was director of group technology strategy, STATS ChipPAC. He also worked deputy lab director of MMC (Microsystem, Module and Components) lab, IME (Institute of Microelectronics), A*STAR, Singapore. "YOON" received Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds MBA degree from Nanyang Business School, Singapore. He has over 300 journal papers, conference papers and trade journal papers, and over 20 US patents on microelectronic materials and electronic packaging. Currently working as technical committee member of various international packaging technology conferences, EPTC, ESTC, IMAPS, IWLPC and SEMI.*
8:45am-9:30am	KEYNOTE 4: ***GET MOoRE OUT OF THE PACKAGE*** *The expectation of what progress must be achieved node-to-node in semiconductor scaling is quite clear: follow Moore's Law. However, this alone will not suffice in enabling the next generation products our industry demands. Products are not simply isolated chips: chips need to integrate into a complex system of components. Package Integration is the main enabler to more functionality, more data, and higher speed at a product level. This presentation will investigate what it is we need to get out of the package in order to continue supporting solutions for next generation products.* *Dr. Wolfgang Sauter, Customer Engineering Solutions – Packaging, Marvell Semiconductor* *Wolfgang Sauter is a Principal Engineer at Marvell's newly acquired ASIC Business Unit. He works on advanced package solutions and chip interface definition for all ASIC products that require integration of multiple active components. Before he started at Marvell Semiconductor, Wolfgang worked as a Packaging Engineer at IBM, and as a Customer Product Solutions Architect at Globalfoundries and at Avera Semi. Wolfgang has authored more than 30 industry papers and publications, and holds more than 120 patents.*
9:30am-9:45am	*Break in the Foyer*

FOUNDATION GOLF OUTING AT 1:30PM
at WeKoPa Golf Course (Cholla Course)

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BEFORE TUESDAY, MARCH 3 AT 12pm

	3D INTEGRATION Track ROOM 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track ROOM 104-106	ADVANCED PACKAGING & EMERGING MATERIALS for AUTOMOTIVE, 5G & NEXT GEN APPLICATIONS Track ROOM 102-103
THURSDAY MORNING SESSIONS:	TH-AM1: BONDING & METROLOGY Chair: Mike Kelly, Amkor Technology; Steffen Kröhnert, ESPAT-Consulting	TH-AM2: NOVEL CONCEPTS IN FAN-OUT & WAFER LEVEL PACKAGING Chairs: Chris Scanlan, JCET Group; Linda Bal, TechSearch	TH-AM3: NEXT GEN APPLICATIONS Chairs: YongJai So, Amkor Technology; Tu-Anh Tran, NXP Semiconductors
9:45am-10:15am	044 *Paths towards Ultra High-Density Interconnect 3D Systems: Contribution of Wafer Geometry for Achieving sub 200nm Wafer-To-Wafer Bonding Overlay* Serena Iacovo, IMEC (Joeri De Vos, Alain Phommahaxay, Andy Miller, Eric Beyne, Thomas Uhrmann, Andreas Fehkuhrer)	022 *Polymer Enabled Ultra-thin Package Solutions for Heterogeneous, Package-in-package and Embedded ICs* Doug Hackler, American Semiconductor (Chris Milasincic, HD MicroSystems; Ed Prack, MASIP LLC)	009 *High Density Integrated Stack Capacitor (ISC) for Advanced Package Solutions* Max Min, Jaejune Jang, Samsung Foundry (Sugmin Hong, Jaeyup Chung, Yoojeong Jeong, Sunwoo Park, Jihyung Kim)
10:15am-10:45am	051 *Collective D2W Hybrid Bonding for 3D SIC and Heterogeneous Integration* Thomas Uhrmann, EV Group (J. Burggraf, M. Pires)	025 *Heterogeneous System-in-Package (HSIP) Using Fan-Out Wafer-Level Packaging (FOWLP)* Charles Woychik, i3 Microsystems, Inc. (Justin Borski, Robert Nead)	015 *Development of Additive Technology for Advanced Packaging* Jason Rouse, Sekisui Products LLC (Takanori Inoue, Taichi Hamada, Yusuke Fujita, Yoshifumi Sugisawa, Mitsuru Tanikawa, Takashi Watanabe)
10:45am-11:15am	055 *A Novel Permanent Bonding Material* Reihaneh Sejoubsari, Brewer Science (Xiao Liu, Trevor Stanley)	035 *Design Rule Study of Low Pressure Compression Molding Process on Polymer Cavity Packages* Nao Honda, Nippon Kayaku Co., Ltd.	017 *Autocatalytic Tin - How to Overcome Process Limitations to Introduce a New Solution for Thick Tin Plating* Sandra Nelle, Atotech Deutschland GmbH (B. Schafsteller, K. Tuna, G. Ramos)
11:15am-11:45am	034 *Improved Optical Profiler Metrology for Advanced Packaging* Samuel Lesko, Bruker - Nano Surfaces	049 *Glass based Panel Fanout Packaging for High-Frequency Applications* Siddharth Ravichandran, Georgia Institute of Technology (Atom Watanabe, Nobuo Ogura, Rao Tummala, Madhavan Swaminathan)	026 *Online Monitoring of Panel Level Packaging Process Solutions* Michael Pavlov, ECI Technology (Karsten Andra, William Finck, Jinjing Wang, Eugen Shalyt, Paul Okagbare, Vishal Parekh, Michael MacEwan)
11:45am	*Conference Ends*		

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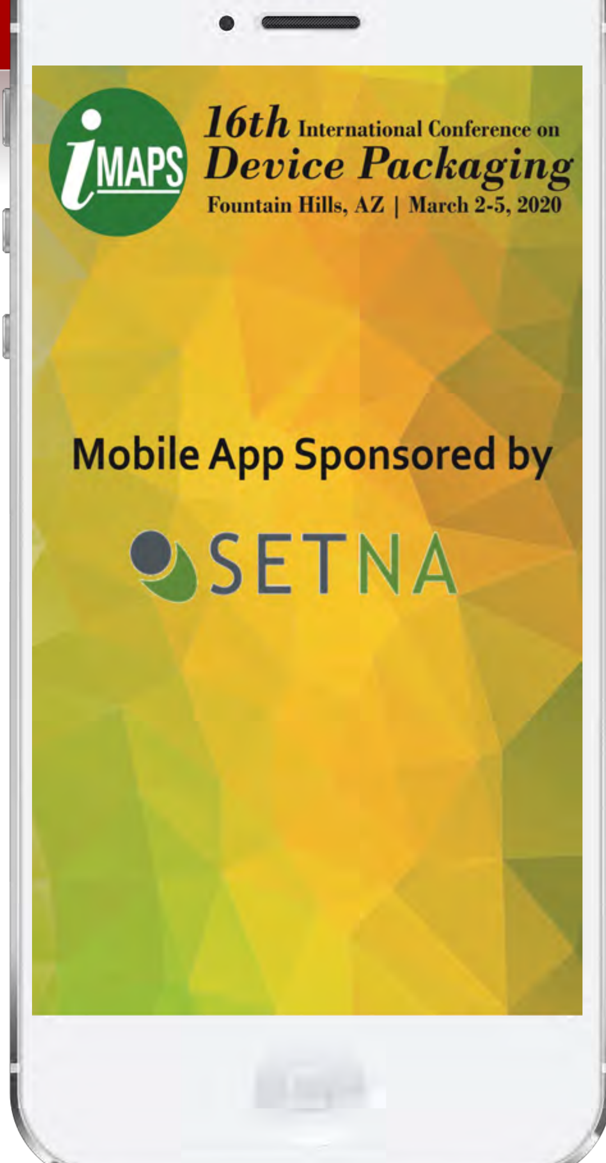

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