FINAL PROGRAM

19TH INTERNATIONAL CONFERENCE & EXHIBITION ON

DEVICE PACKAGING

FOUNTAIN HILLS, AZ

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MARCH 13-16, 2023

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ASE

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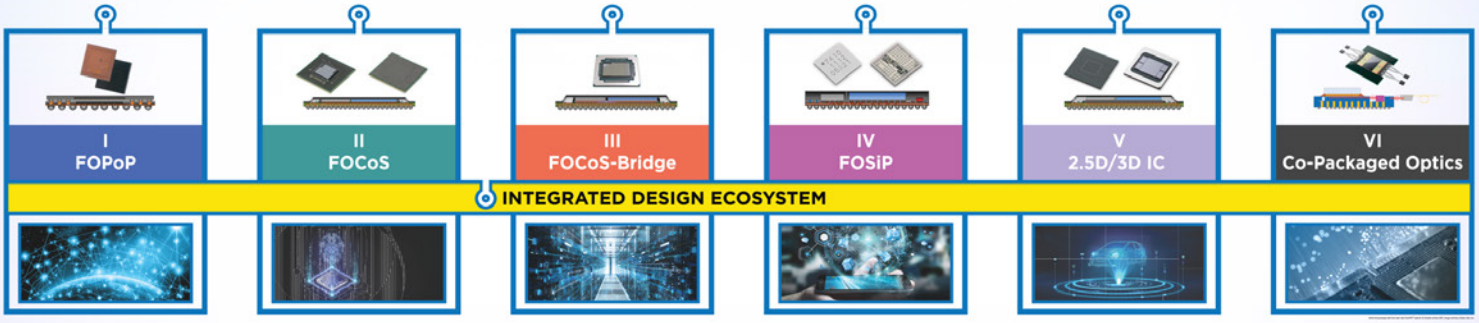

"Our expanding digitized world is driving unparalleled innovation across the semiconductor industry and VIPack™ represents a crucial leap forward in the transformational packaging technologies required to achieve the highly complex system integration our customers need to remain competitive," said Yin Chang, Senior Vice President of Sales and Marketing. "Through VIPack™, we're empowering our customers to discover new efficiencies in their semiconductor design and manufacturing process and to reimagine the integration technologies required to accomplish application excellence."

"ASE is delighted to bring its VIPack™ platform to market, opening up new opportunities for our customers to innovate from the design process all the way to production and to reap extensive benefits in relation to functionality, performance, and cost," said Dr. C.P. Hung, Vice President of R&D, ASE. "As the world's leading OSAT, ASE is strategically positioned to help customers improve efficiency, speed time-to-market, and sustain profitable growth. VIPack™ underscores our commitment to deliver our most innovative packaging technologies to date."

Available now, ASE's VIPack™ is a scalable platform that will expand in alignment with industry roadmaps

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Welcome from the General Chair

Welcome to the Device Packaging Conference (DPC) 2023!

I feel exceptionally pleased to welcome everyone to DPC 2023. This annual conference has been a part of the semiconductor industry for many years now and has been instrumental in yielding useful and spectacular results.

2023 will certainly be an interesting year for the world, as Covid-19 is no longer declared an emergency in the US and most other countries. The Covid-19 pandemic has had an unexpected economic impact throughout the globe. Over the last three years, we saw the largest economic decline followed by the fastest recovery in many decades in every market segment including semiconductors. Now the world economy is poised to slow this year, before an expected rebound next year. Growth is expected to be weak as inflation and Russia's war in Ukraine remain ongoing.

IMAPS DPC 2023 presents over 80 of our industry's most knowledgeable experts sharing the latest packaging solutions for today's and future challenges. I am honored to chair this year's conference, which has an impressive program that includes 12 PDCs by industry and academic experts, 4 keynote addresses, a GBC plenary session on research to manufacturing discussion, an evening panel discussion on packaging chiplets, 3 technical tracks, an IMAPS/3D InCites Roundtable Discussion on Diversity, Equity, and Inclusion (DEI): It Takes a Village, plus a poster session covering key application areas like AI, Automotive, and 5G/6G along with the latest Wafer Level Packaging, Flip Chip, SiP/HI, 2D/3D, and chiplet packaging solutions.

We are happy to see everyone again at the We-Ko-Pa Conference Center in beautiful Fountain Hills, AZ. Be sure to visit the sold-out exhibit hall to see the latest on display from industry-leading vendors.

Nokibul Islam
JCET Group

Access the Device Packaging *MOBILE APP*

Conference App Sponsored By

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The mobile app is the exclusive source for all speaker extended abstracts, PLUS:

- The *full* conference program & updates
- Session descriptions
- Searchable attendee list
- Searchable exhibitor list
- Info, Links, and News
- Personal conference schedule

Here's how to get the app

1. Visit the Apple Store or the Google Play store and search "IMAPS Events" or visit https://imaps.gatherdigital.com for the web-based version.
2. Log in with your registration email and the password dpc2023.
3. Take advantage of all of the attendee and exhibitor features!

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Professional Development Courses (PDCs)

Course Fees: $425 per course. Fees include access to the 2-hour course led by reputable industry leaders. Attendees may select up to one course in each time slot. These fees are non-refundable but may be transferred to another registrant prior to the start of the course. No transfers will be accepted once the course has begun.

Monday, March 13	Professional Development Courses (PDCs)		
7:00am – 7:00pm	**REGISTRATION** Wasaja Ballroom Foyer		
MORNING Professional Development Courses (PDCs) – 8:00am-12:30pm			
	Wassaja Conf Room 104	Wassaja Conf Room 105	Wassaja Conf Room 106
8:00am – 10:00am 2-HOUR FORMAT	**PDC1: The Evolution of Flip Chip Package Technology** Mark Gerber, ASE US, Inc.	**PDC2: Packaging Processes, Materials, Quality and Reliability** Syed Sajid Ahmad, Consultant	**PDC3: Chiplet Design and Heterogeneous Integration Packaging** John Lau, Unimicron
10:30am – 12:30pm 2-HOUR FORMAT	**PDC4: Introduction to Fan-Out Wafer Level Packaging (FOWLP)** Beth Keser	**PDC5: Wire Bond Process Optimization** Henri Seppaenen, Kulicke & Soffa Industries	**PDC6: 5G/6G/mmWave Materials, Test and Packaging Development Requirements** Urmi Ray, iNEMI
12:30pm – 1:00pm	LUNCH (boxed lunches can be picked up in the foyer from 12-12:30pm) Only provided for those attendees registered for BOTH Morning and Afternoon PDCs		
AFTERNOON Professional Development Courses (PDCs) – 1:00pm-5:30pm			
	Wassaja Conf Room 104	Wassaja Conf Room 105	Wassaja Conf Room 106
1:00pm – 3:00pm 2-HOUR FORMAT	**PDC7: Polymers for Wafer Level Packaging** Jeff Gotro, InnoCentrix, LLC	**PDC8: Failure Analysis in Semiconductor Package Assembly** Tom Dory, Fujifilm Electronic Materials USA	**PDC9: System-in-Package (SiP) - System Solutions Through Miniaturization** Mark Gerber, ASE US, Inc.
3:00pm – 3:30pm	COFFEE BREAK IN FOYER		
3:30pm – 5:30pm 2-HOUR FORMAT	**PDC10: Fan Out for Advanced Packaging Application** John Hunt, TechSearch International	**PDC11: Thermal Challenges and Opportunities of Advanced Packages and Microelectronics Systems** Victor Chiriac, Global Cooling Technology Group	**PDC12: Semiconductors in Automotive - Technology Trends and Reliability** Vikas Gupta, ASE US, Inc.; Pradeep Lall, Auburn University
5:30pm – 7:00pm	**WELCOME RECEPTION** Wassaja Conference Room 107-108 Followed by the **DEI Roundtable** **NEW at DPC this Year** **(All Attendees are invited to attend)**		
7:00pm – 8:00pm	**IMAPS/3D InCites DEI Roundtable Discussion on:** **DEI: It Takes a Village** Wassaja Conference Room 107-108 ***See page 6 for a complete description of this new event!***		

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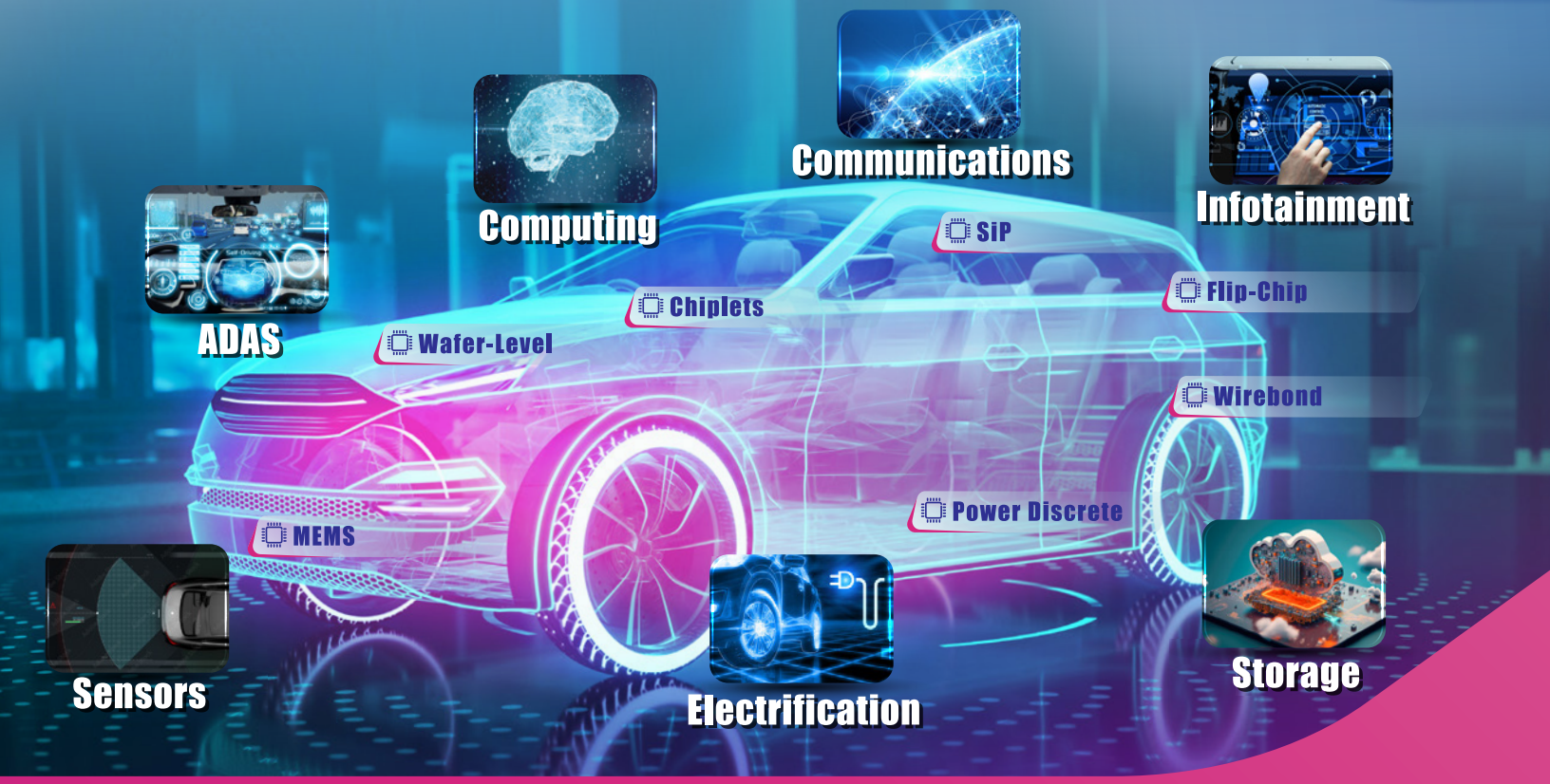

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Design

- Chip-Package Co-Design
- RF SiP Design and Antenna Simulation
- Fast, Efficient Design Process
- Thermal, Electrical & Mechanical Characterization

Assembly

- Wire Bond Operations
- Flip Chip with On-Site Bumping Operations
- Wafer Level Processing
- SiP & AiP Integrations

Test

- Wafer, RF, Final & System Level Test
- RF, Mixed-Signal, Digital, HPC & High-End Memory Applications
- Test Program Development
- Data Collection & Yield Analysis

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IMAPS/3D InCites DEI Roundtable Discussion on:

DEI: It Takes a Village

Wassaja Conference Room 107-108

New this year!

DEI Chair:
Robin Davis, Deca Technologies

Moderator & Podcaster:
Françoise von Trapp, 3D InCites

Panelists:
Francesca Domingo, EMD Group,
Head of University Relations & Talent Strategy, EMD Group

Ann McKenna, Arizona State University,
Fulton Schools of Engineering
Vice Dean for Strategic Advancement

Rebeca Obregon-Jimenez, Avnet
SVP Strategic Business Engagements & Supplier Management

Robin Stubenhofer, Kansas City National Security Campus (KCNSC) managed by Honeywell
VP of Engineering

The target audience is not HR or hiring managers, but the regular attendees who may be wondering what they can do to help create an atmosphere of equity and inclusion at their work place. We want to ask the hard questions that people might be asking: Why should I care? Why do I need to use my pronouns? What can I do/say to have an impact on our company culture?

Diversity:

Includes but is not limited to race, color, ethnicity, nationality, religion, socioeconomic status, veteran status, education, marital status, language, age, gender, gender expression, gender identity, sexual orientation, mental or physical ability, genetic information, and learning styles.

Equity:

The guarantee of fair treatment, access, opportunity, and advancement for all while striving to identify and eliminate barriers that have prevented the full participation of some groups. The principle of equity acknowledges that there are historically under-served and under-represented populations and that fairness regarding these unbalanced conditions is needed to assist equality in the provision of effective opportunities to all groups.

Inclusion:

Authentically bringing traditionally excluded individuals and/or groups into processes, activities, and decision/policy making in a way that shares power and ensures equal access to opportunities and resources.

IMAPS aSIP is now CHIPcon!

The top global event for Chiplet and Heterogeneous Integration Packaging (CHIP), covering advanced technology developments and solutions, device integration strategies, and business trends.

IMAPS has rebranded its well-attended, annual Advanced System-in-Package conference to the Chiplet & Heterogeneous Integration Packaging Conference CHIPcon. As the world's leading semiconductor companies continue to push the edge of process technology, the industry is seeing a marked shift in device design and architectures to overcome economic and time-to-market challenges. The conference name change is the result of the rapidly rising adoption of chiplet based device architectures, and the increasingly critical role packaging technology is taking in the manufacture and enablement of these advanced products.

The IMAPS CHIPcon conference will focus exclusively on innovative device integration technology developments, solutions, and business trends. CHIPcon 2023 will offer cutting-edge presentations from scientists, technologists and business leaders across the globe in cellular, IoT, automotive, high-performance computing and networking market segments.

Advanced CHIP technology is an umbrella term to cover a variety of packaging technology subsets, including laminate/glass/ ceramic/silicon/leadframe based SiP, FanOut RDL, 2.5D/3D Heterogeneous Integration, and modules.

The conference will explore the current state of the art and emerging packaging technology roadmap supporting the integration and delivery of a complete system or subsystem solution. Attendees will be exposed to thought-provoking advanced package structures with high functioning system performance, mechanical reliability, thermal management and high yield manufacturability.

July 24-27, 2023

DoubleTree by Hilton San Jose

CHIPcon speaker opportunities are by invitation-only from the technical committee.

Professional Development Courses (PDCs)

Following are descriptions of the 12 Professional Development Courses.
See page four for the complete schedule.

PDC1:
The Evolution of Flip Chip Package Technology

Mark Gerber, ASE US, Inc.

This PDC course will provide a historical overview and background on the evolution of flip chip packaging as well as short market perspective on this platform. Mobile, Infrastructure, Automotive, High Reliability, Medical and High-Performance Network and Computing all rely on Flip Chip technology to enable their silicon solutions. Although the use of new technologies such as Fan-Out hold promise for certain applications, flip chip advancements continue to challenge many new technology competitors from a price and reliability perspective and may end up driving hybrid approaches. Interconnect structure, process flows, materials and package integration process methods for evolving Flip Chip applications will be discussed in detail. Understanding the trade-offs between the different bump structures and package platforms is key in determining the silicon device layout and the type of design rules that can be leveraged for new products. As part of this course, the assembly process details will be discussed and will include Mass Reflow, Thermo-Compression Non-Conductive Paste (TCNCP) bonding, Laser Assisted Bonding, and Hybrid Bonding. Reliability aspects such as IMC formations and ways to address will also be covered as a key consideration for Interconnect decisions.

PDC2:
Packaging Processes, Materials, Quality and Reliabiity

Syed Sajid Ahmad, Consultant

The course presents manufacturing, materials, quality and reliability info in terms understandable to engineering and non-engineering personnel. Packaging characteristics and drivers will be outlined. Types of packages and critical differences among them and their applications will be discussed. The course will look at the design selection to meet use and application environments. Step-by step manufacturing flow for plastic packages will be presented as an example to understand the complexity of processes, materials and equipment involved in their manufacture. Advanced packaging will be introduced. Materials selection with respect to application environments will be discussed. Quality and reliability issues related to chip packaging and assembly and their solution will be outlined.

PDC3:
Chiplet Design and Heterogeneous Integration Packaging

John Lau, Unimicron

Chiplet is a chip design method and heterogeneous integration (HI) is a chip packaging method. HI uses packaging technology to integrate dissimilar chips, photonic devices, and/or components (either side-by-side, stacked, or both) with different sizes and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem on a common package substrate. For the next few years, we will see more implementations of a higher level of chiplet designs and HI packaging, whether it is for time-to-market, performance, form factor, power consumption or cost. In this lecture, the introduction, recent advances, and trends in chiplet design and HI packaging will be presented. The contents are: (1) Introduction; (2) System-on-Chip (SoC); (3) Chiplet Design and HI Packaging; (4) Advantages and Disadvantages of Chiplet Design and HI Packaging; (5) AMD Chiplet Design and HI Packaging: (a) EPYZ and (b) RYZEN; (6) Intel Chiplet Design and HI Packaging: (a) FOVEROS, (b) FOVEROS Direct, and (c) Ponte Vecchio; (7) TSMC chiplet Design and HI Packaging: (a) SoIC, (b) SoIC + CoWoS, and (c) SoIC + InFO PoP; (8) Chiplets Lateral Interconnects (Bridges): (a) Intel's EMIB, (b) IBM's solution for EMIB, (c) Applied Materials' Bridge Embedded in Fan-Out EMC, (d) SPIL's FO-EB, (e) TSMC's LSI, (f) ASE's sFOCoS, (g) IME's EFI, (h) Amkor's S-Connect Fan-Out Interposer, and (i) UCIe; (9) HI Packaging on Organic Substrates: many examples; (10) HI Packaging on Silicon Substrates (TSV-Interposers): many examples: (a) Leti, (b) IME, (c) HKUST, (d) ITRI, (e) Xilinx/TSMC, (f) Altera/TSMC, (g) NVidia/TSMC, (h) AMD/UMC, (i) AMD's Active Interposer, (j) Intel's FOVEROS, (k) TSMC's SoIC, and (l) Samsung's X-Cube; (11) HI Packaging on Silicon Substrates (TSV-Less Interposers) such as Bridges; (12) HI Packaging on Ceramic Substrate: one example; (13) HI Packaging on Fan-Out RDL (Organic Interposers) for High Performance Applications: many examples: (a) STATSChipPac's FOFC-eWLB, (b) ASE's FOCoS, (c) MediaTek's FO-RDLs, (d) TSMC's InFO_oS and InFO_MS, (e) Samsung's Si-Less RDL Interposer, (f) TSMC's RDL-Interposer, (g) ASE's FOCoS (Chip-Last), (h) Shinko's Organic RDL-Interposer, and (i) Unimicron's Hybrid Substrate; (14) Assembly Technologies for Chiplet Design and HI Packaging: (a) SMT, (b) Solder Bumped Flip Chip, (c) CoW, (d) WoW, (e) TCB, and (f) Bumpless Cu-Cu Hybrid Bonding; and (15) Trends in Chiplet Design and HI Packaging.

Professional Development Courses (PDCs)

PDC4:
Introduction to Fan-Out Wafer Level Packaging (FOWLP)

Beth Keser, IMAPS President

Fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for over 10 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wirebond and bump interconnections, substrates, leadframes, and the traditional flip chip or wirebond chip attach and underfill assembly technologies across multiple applications. This course will cover the advantages of FO-WLP, potential application spaces; package structures available in the industry; materials, equipment and process challenges; and reliability.

Course outline:

- Current Challenges in Packaging
- Definitions and Advantages
- Applications
- Package Structures
- Materials
- Equipment
- Design Rules & Reliability

PDC5:
Wire Bond Process Optimization

Henri Seppaenen, Kulicke & Soffa Industries

This wire bonding professional development course provides deep dive into wire bonding technologies, techniques, process development, and optimization. The course will introduce wire bonding technologies from thin wire ball bonding and large wire wedge bonding to heavy ultrasonic copper ribbon bonding. After the introduction, we present wire bonding fundamentals, the physics of bonding, and material science to understand the bonding process, process optimization, and reliability. We share practical methods for the wire bond process optimization, including parameter selection, destructive and non-destructive testing, and how to use analysis tools such as trace analysis, DOE, and response surface. The course will also highlight the recent advances in wire bonding technology and process development. This course is for anyone who wants to learn or deepen their understanding of wire bonding. Beginners will get practical information on how to improve the bonding process and seasoned professionals will get in-depth science-based knowledge in wire bonding, including references and links to the source materials.

PDC6:
5G/6G/mmWave Materials, Test and Packaging Development Requirements

Urmi Ray, iNEMI

Millimeter-wave (mmWave) frequencies unlock the true potential of 5G. The ultra-wide bandwidths enable faster wireless connection speeds and high capacity with low latency, providing the ideal solution to meet increasing industry and government demands. Many mobile network operators started deploying commercial 5G mmWave networks in 2020. All have massive mmWave deployment plans on their roadmaps. In response, 5G chipset, device, and base station makers are ramping up their design and manufacturing powers to bring more 5G mmWave services to market. It should be noted that 5G requires a complex new ecosystemThe key to enabling this architecture is packaging and system integration, especially involving an effective antenna structure and RFIC communication in cost-effective, small form-factor packages. As full speed development, demonstration and qualification of mmWave systems have accelerated in this decade, different design and packaging architectures are emerging.

This PDC will cover two major topics: (1) Industry roadmapping activities summarizing the technology needs in materials, material characterization and electrical test and (2) integration and packaging options providing a comprehensive landscape of package development including FOWLP as well as laminate/glass based packaging. The specific requirements of materials and process needs (low dielectric material, copper roughness requirements) will be discussed. Product application spaces ranging from mobile/handheld to network infrastructures and automotive/satellite radars are highlighted. Key aspects and guidelines towards a cost/performance trade-off analysis will be summarized.

Professional Development Courses (PDCs)

PDC7:
Polymers for Wafer Level Packaging

Jeff Gotro, InnoCentrix, LLC

The course has been completely updated to include a detailed discussion of the polymers and polymer-related processing for Fan-Out Wafer Level (FOWLP) packaging as well as Fan-Out Panel Level packaging (FOPLP). The course will provide an overview of the important structure-property-process-performance relationships for polymers used in wafer level packaging. The main learning objectives will be:

1) Gain insights on how polymers are used in Fan Out Packaging, specifically mold compounds and polymer redistribution layers (RDL)

2) Understand the key polymer and processes challenges in Fan Out Wafer Level Packaging

3) Learn about polymers and processes used in Fan Out Panel Level Packaging including new materials for mold compounds and a detailed description of the polymers used for RDL in FOPLP.

Course Topics:

- Overview of polymers used in Wafer Level Packaging
- Wafer level process flows (chip first versus chip last (RDL first))
- Epoxy Mold compounds for eWLP
- Photosensitive polyimides and polybenzoxazoles
- Polymer reliability challenges in Fan-out wafer level packaging
- Processes and materials for Fan Out Panel Level Packaging
- Wafer versus panel processing; polymer challenges and solutions

Professional Development Courses (PDCs)

PDC8:
Failure Analysis in Semiconductor Package Assembly

Tom Dory, Fujifilm Electronic Materials USA

The objective of this PDC is to provide the participants with an overview of the technologies, materials, and processes involved in the latest assembly failure analysis methods.

PDC participants will receive a detailed review of failure analysis methods and reliability testing in assembly. Quickly finding and eliminating package defects and failures due to assembly issues is critical. Package reliability directly affects manufacturing yield, time to market, product performance, customer satisfaction and cost. Many process steps and controls are needed for a high yield and reliable assembly process. A thorough understanding of product and technology reliability principles and mechanisms of failure is essential. Knowledge of defects and failure mechanisms enables a high yielding successful assembly process through material choices, package design, process optimization, and thermo-mechanical considerations. Fault isolation, failure analysis, and materials analysis play a major role in the improvement of yield and reliability. Coordination of engineers from many disciplines is needed in order to achieve high yield and reliability. Each engineer needs to understand the impact of their choices and methods on the final product. This workshop will discuss, using examples, mechanical and thermal failure mechanisms in assembly and detection methods.

PDC9:
System-in-Package (SiP) - System Solutions Through Miniaturization

Mark Gerber, ASE US, Inc.

This PDC course will introduce the package platform SiP (System-in-Package) and how some companies are diversifying from SOC (System-on-a-Chip) to leverage heterogeneous silicon integration and package miniaturization to enable system level solutions. A short market perspective will be reviewed as well as how industry segments are leveraging SiP and how the OEM market is evolving and creating system level ecosystems to enabling content revenue- a key area of IOT. SiP general process flow details will be covered as well as key process considerations for yield improvements. In addition, a brief overview of some of the tools that may be leveraged to help miniaturize module solutions and improve performance. This class will also introduce several variations of the SIP platform using Fan-Out Wafer Level packaging and new embedded substrate technologies are also emerging as powerful future platforms to enable lower power and higher performance devices using solderless interconnects.

PDC10:
Fan Out for Advanced Packaging Applications

John Hunt, TechSearch International

Fan Out technology has evolved as alternative packaging to meet both the need for miniaturization of electronics, using low density Fan Out, and for the complex interconnectivity of complex packages using more advanced Fan Out assemblies.

The increased use of Mobile and IOT for communication and entertainment has driven the need for increased capability of data centers. Fan Out technology is currently used for many of these applications. It has enabled the heterogeneous integration of die and memory with improved electrical performance and lower cost than traditional 2.5 packaging for data center requirements.

We will review how wafer level processing technologies, the evolution of substrate technologies, and Flip Chip packaging have combined to enable advances in Fan Out packaging. These structures are used for a variety of automotive, IoT, advanced mobile, server and AI applications. They allow for higher levels of integration and sophistication than has been possible in the past with traditional packaging techniques.

A brief overview of the concept of Fan Out packaging, the history of its evolution, followed by more detailed discussions of recent Fan Out developments for advanced applications, including the integration of chiplets into complex packages is included in this course.

PDC11:
Thermal Challenges and Opportunities of Advanced Packages and Microelectronics Systems

Victor Chiriac, Global Cooling Technology Group

The digital world requires higher performance, more data and faster processors. Heterogeneous Computing involves innovative packaging solutions for the central processing units (CPUs), the graphics processing units (GPUs), high speed interconnects and other elements that enable superior computing. The emergence of 5G/6G leads to significant rise in mobile communication, IoT technology and beyond, providing the infrastructure needed to carry huge amounts of data, allowing for a smarter and more connected world. This course will highlight the current and future thermal challenges and opportunities spanning from the package to the system level, impacting the small to large electronics and other advanced systems of the future.

Professional Development Courses (PDCs)

PDC12:
Semiconductors in Automotive - Technology Trends and Reliability

Vikas Gupta, ASE US, Inc.

The first part of the PDC will provide a summary of key disruptive trends in automotive electronics in the upcoming years. The increased emphasis on autonomous driving as well as electrification of vehicles has resulted in enormous changes for semiconductors and packaging. Following megatrends will be discussed

- Autonomous
  - Introduction of advanced nodes and packages for processors
  - Sensing technologies
- Electrification
  - Power systems trend
  - Wide band gap implementation

In the second part of this professional development course, the design, materials, and reliability strategies for automotive electronics will be presented. Electronics are increasingly being used in automotive platforms for a variety of mission-critical and safety-critical activities, such as guidance, navigation, control, charging, sensing, and operator interaction. Over the last two decades, automotive platforms have expanded to incorporate hybrid and fully-electric vehicles. Much of the electronics is located under the car's hood or in the trunk, where temperatures and vibration levels are far higher than in consumer office applications. During the vehicle's use-life, electronics in the automotive underhood may be exposed to sustained high temperatures of 125-150C for extended periods of time. The automotive electronics council (AEC) has graded electronics for automotive purposes into four categories: grade-0, grade-1, grade-2, and grade-3. Grade-0 components have the most demanding criteria of the four grade categories, with predicted power temperature cycling ranging from -40C to +150C for 1000 cycles and ambient temperature cycling ranging from -55C to +150C for 2000 cycles. Furthermore, the grade-0 components are expected to be capable of sustaining high-temperature storage for 1000 hours at 175C. With the introduction of new packaging architectures, the area of packaging applications has continued to evolve, allowing for powerful computing on mobile automobile platforms. New materials and integration technologies have also emerged, allowing for tighter integration of electronics sensing and processing into the structural characteristics of the vehicle. The automobile platform faces a series of constraints particular to the real-time context for enabling sophisticated functionality.

Device Packaging Technical Sessions

Tuesday, March 14

7:00am-7:00pm Registration Wasaja Ballroom Foyer

7:00am-8:00am Continental Breakfast Sponsored by:

8:00am-8:20am OPENING COMMENTS Wassaja Conference Room 107-108
General Chair: Nokibul Islam, JCET Group

Plenary/Keynote Session Sponsored by:

Tuesday, March 14 Keynote Session

8:20am-9:05am

KEYNOTE 1 Wassaja Conference Room 107-108

CHALLENGES FOR THE NEXT GENERATION OF PACKAGE TECHNOLOGY AND INTEGRATION

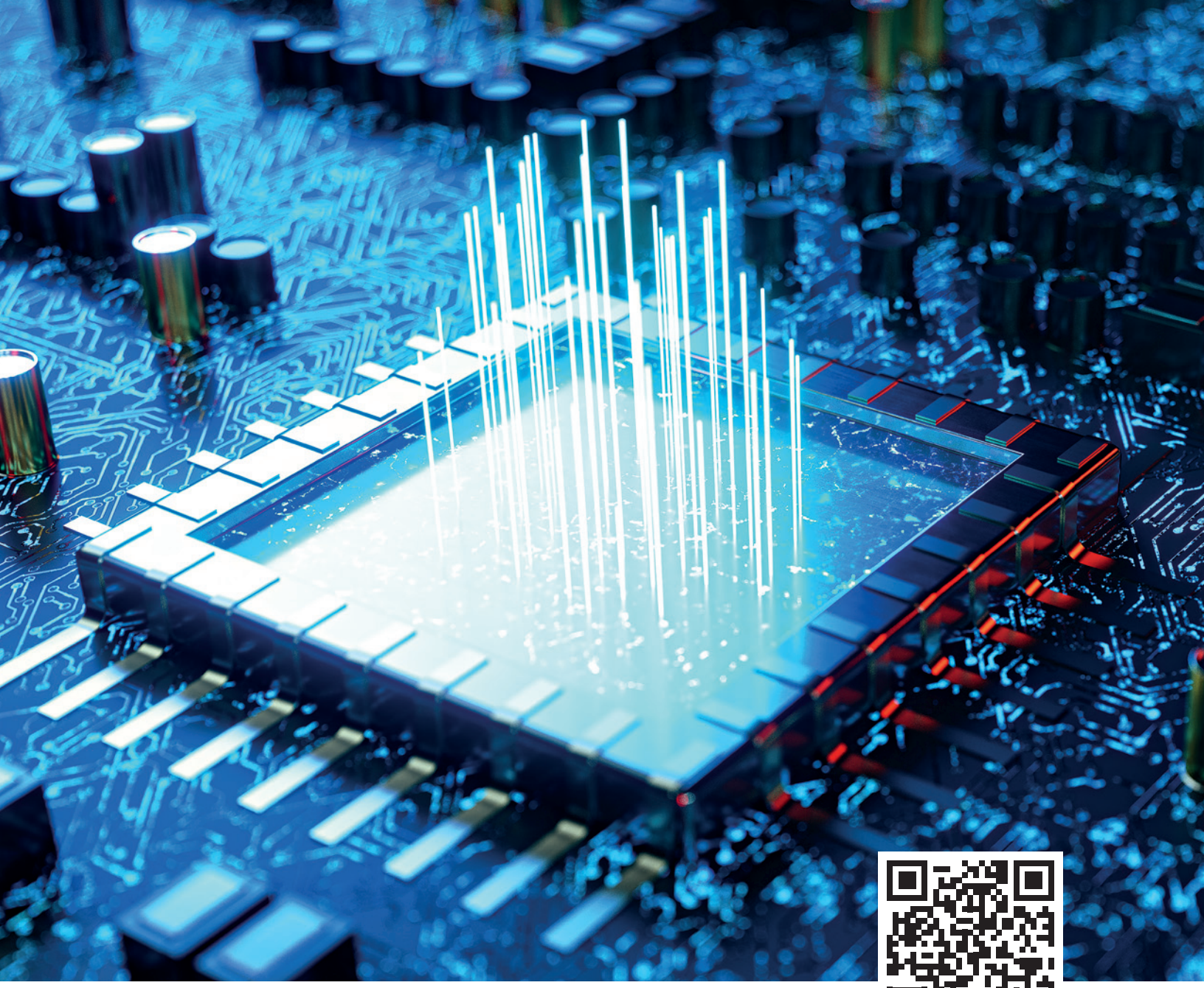
Ahmer Syed, Qualcomm Technologies, Inc.

With Moore's Law slowing down, advanced packaging solutions are required to optimize a cost-performance matrix. There is a greater need now than ever before for looking at alternate packaging solutions. The task is especially challenging for mobile application where package size and thickness still puts significant constraints on technology options. Similarly, system design and integration continue to put barriers for innovation in a non-vertically integrated supply chain business model.

This presentation highlights these challenges and discusses some of the ways to overcome these with packaging playing a critical and central role.

Ahmer Syed *is a VP of Engineering at Qualcomm in Global Manufacturing Technology and Operations organization. He leads a global team responsible for packaging technology development, NPI, HVM deployment for 5G, mobile, IoT, Connectivity, Automotive, and Computer markets.*

A 30+ year veteran of the Semiconductor and electronics industries, Ahmer has extensive experience in developing advanced packaging technologies such as Flip Chip, WLCSP, FO-WLP, Package on Package (PoP), QFN, MEMS and System in Package (SiP). He has authored and contributed to more than 70 technical papers and articles on advanced packaging and reliability and has been a keynote speaker at various international conferences.



SUSS EQUIPMENT SOLUTIONS FOR NEXT-GENERATION PACKAGING TECHNOLOGIES

SUSS MicroTec is a leading supplier of equipment and process solutions for the semiconductor industry enabling state-of-the-art packaging technologies from R&D to high volume production.

With landmark lithography solutions for FOWLP and leading edge wafer bonding technologies for 2.5D and 3D stacking, we contribute to the advancement of packaging and system integration.

Always be one step ahead — with solutions from SUSS MicroTec.
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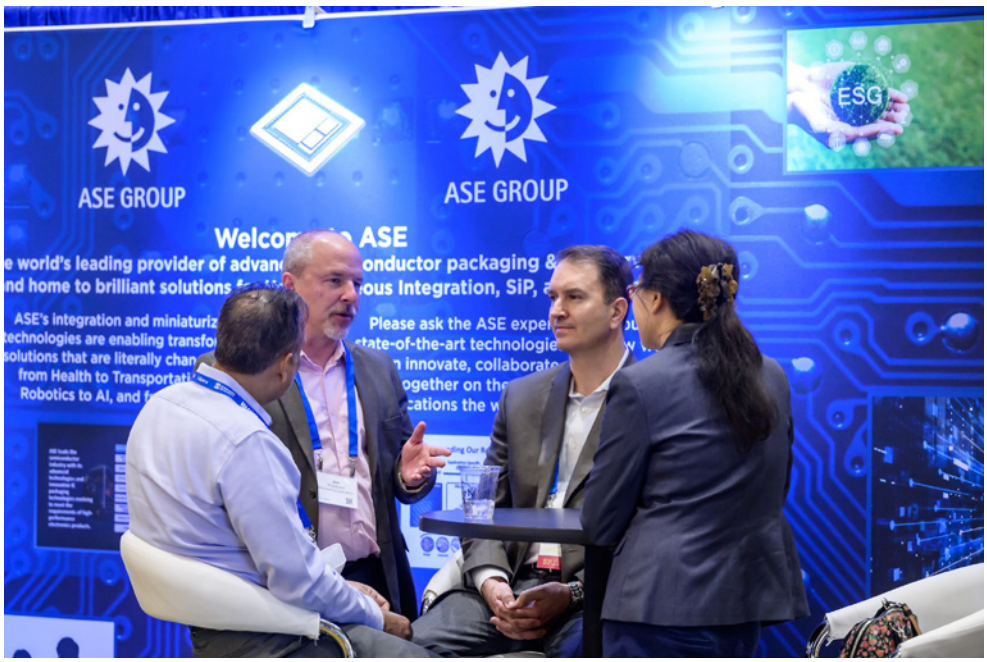
SUSS MicroTec

Device Packaging Technical Sessions - *Tuesday continued*

Tuesday, March 14 Keynote Session

9:10am-9:55am	**KEYNOTE 2** Wassaja Conference Room 107-108 **ADVANCED PACKAGE SOLUTIONS IN AI/ML AND DATA ERA** **Seungwook "Stewart" Yoon, Samsung Electronics** High-performance chip size continues to increase up to one reticle size and the cost of the leading-edge silicon node is soaring. Ongoing increases in performance requirements from Cloud to Edge to on-premise use cases require tighter coupling of computer, memory and storage resources. And higher bandwidth and density solutions are important for high-end systems. So memory coherency and low latency attributes across converged computer infrastructures with interconnect technologies including UCIe (Universal Chiplet Interconnect Express). Advanced package solutions (FOPKG , 2.xD, 3D, 3.5D) are to be introduced and discussed in terms of challenges and opportunities for emerging high-end computing, memory and mobile platforms. **Seungwook Yoon** *is currently working as Corporate VP/Head of Team of Package Solution Planning and Strategy, Samsung Electronics.* *Prior to joining Samsung, He was director of group technology strategy, STATS ChipPAC, JCET Group. He also worked as deputy lab director of MMC (Microsystem, Module and Components), IME (Institute of Microelectronics), A*STAR, Singapore. YOON received his Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds a MBA degree from Nanyang Business School, Singapore. He has over 300 journal papers, conference papers and trade journal papers, and over 20 US patents on microelectronic materials and electronic packaging. He has served as technical committee member of various international packaging technology conferences, EPTC, ESTC, IMAPS, IWLPC and SEMI.*
9:55am-10:15am	**Conference Leadership Recognition & 3D InCites Awards** General Chair: Nokibul Islam, JCET Group Awards: Francoise von Trapp, 3D InCites
10:00am-6:30pm	**EXHIBITIONS OPEN** Wasaja Ballroom
10:15am-10:45am	Break in the Exhibit Hall *Sponsored by:* ZESTRON High Precision Cleaning



Device Packaging Technical Sessions - *Tuesday continued*

Tuesday, March 14

	HETEROGENEOUS 2D & 3D INTEGRATION Track Wassaja Conference Room 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track Wassaja Conference Room 104-106	NEXT GEN APPLICATIONS Track Wassaja Conference Room 102-103
TUESDAY MORNING SESSIONS:	**TA1: 2D/3D APPLICATION & TEST** Chairs: Arsalan Alam, AMD; Mollie Benson, NXP Semiconductor	**TA2: DESIGN & TECHNOLOGY** Chairs: Robin Davis, Deca Technologies; Dongshun Bai, Brewer Science	**TA3: iNEMI INVITED SESSION: 5G/6G ROADMAP CREATION AND PACKAGING CHALLENGES** Chair: Urmi Ray, iNEMI
10:45am-11:15am	**Scaling Interconnect Densities to Meet the Growing Demand for Chiplet Integration** Robin Davis, Deca Technologies (Tim Olson)	**Cost Analysis of Fan-out Processes for Chiplet Packaging** Amy Lujan, SavanSys Solutions LLC	**5G/6G MAESTRO Roadmap** Urmi Ray, iNEMI
11:15am-11:45am	**Heterogenous Integration: Simplifying the Landscape** Michael Kelly, Amkor Technology, Inc. (Dave Hiner, George Scott)	**Understanding Warpage Behavior on Different Handling Platforms of FOWLP** Debbie-Claire Sanchez, ERS Electronic GmbH	**Benchmarking 6G Hardware System Design Needs** Markondeyaraj Pulugurtha, Florida International University
11:45am-12:15pm	**Universal Chiplet Interconnect Express™ (UCIe™) - Building an Open Ecosystem of Chiplets for On-package Innovations,** Vik Chaudhry, Amkor Technology	**Thin and Ultra-thin Sidewall Protected P-WLCSP** Doug Hackler, American Semiconductor (Ed Prack, MASIP LLC)	**5G/6G MAESTRO Materials: Glass Substrates for mmWave/sub-THz Applications** Paul Ballentine, Mosaic Microsystems (Shelby Nelson)
12:15pm-12:45pm	**Advanced Test Technologies for Heterogeneous and 2.5D/3D Packaging** Marc Hutner, ProteanTecs (Ken Butler, Advantest Inc)	**Using M-Series with Adaptive Patterning to shrink PCB systems into System-In-Packages** Justin Locke, Siemens EDA (Robin Davis, Deca Technologies)	**5G Electronics: Bridging the Measurement Challenges** Lucas Enright, NIST
12:45pm-2:00pm	Lunch Break in the Exhibit Hall Sponsored by: ASE		

Device Packaging Technical Sessions - *Tuesday continued*

	HETEROGENEOUS 2D & 3D INTEGRATION Track Wassaja Conference Room 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track Wassaja Conference Room 104-106	NEXT GEN APPLICATIONS Track Wassaja Conference Room 102-103
TUESDAY AFTERNOON SESSIONS:	**TP1: PROCESS DEVELOPMENT** Chairs: Suresh Jayaraman, Amkor Technology; Keith Best, Onto Innovation	**TP2: WLP & FLIP CHIP: PROCESS & MATERIALS** Chairs: Jobert van Eisden, MKS/ Atotech; Tim Smith, Nuvotronics	**TP3: PRINTED ELECTRONICS: PROCESSING, DEVICES, AND SYSTEMS** Chairs: Robert Dean, Auburn University; Eric MacDonald, University of Texas, El Paso
2:00pm-2:30pm	**Micro-Textured Film for Immobilizing Bare Die and Packaged Devices During Processing and Handling,** Darby Davis, Gel-Pak	**TIM Materials – Integration and Assembly Aspects in SIP Applications** Kevin Brenner, Southern Methodist University	**Fine-Feature Additively Dry Printed Passive Wireless Sensor Tag** Zabihollah Ahmadi, Auburn University (Masoud Mahjouri-Samani, Robert Dean)
2:30pm-3:00pm	**Assembly Solutions for Cost-Effective Heterogeneous Integration with Disparate Die Types** Glenn Farris, Universal Instruments Corp.	**Liquid Metal Embedded Elastomers as High-performance S-TIM Replacements** Keyton Feller, Arieca (Vivek Singh, Toby Mea, Allyssa Kerr, Jeffrey Gelorme, Navid Kazem, Arieca)	**Development of Electronic Packages with Integrated Environmental Mitigation** Carl Rudd, EngeniusMicro (Peter Zoladz, Greg Poole, Brian English)
3:00pm-3:30pm	**Micro-Transfer Printing for Efficient 3DHI of 100-300mm Wafers and Glass Panels** Bob Conner, X-Celeprint (Bill Batchelor, David Gomez)	**Novel Low Df Thermosetting Film and Photo Imageable Film** Meiten Koh, Taiyo Ink MFG. Co., Ltd	**4D mmW/5G Metasurfaces and Wireless Sensors combining additive manufacturing, morphing and ML technologies** Manos Tentzeris, Georgia Institute of Technology
3:30pm-4:00pm	Break in Exhibit Hall Sponsored by: BRUKER		
4:00pm-4:30pm	**Performance enablement through Advanced FOPOP for Networking and Mobile** Mark Gerber, ASE Group Nathan Whitchurch, Amkor Technology	**Advanced Insulation Materials for Next Generation High-Density Package** Shohei Fujishima, Research Institute for bioscience Products & Fine Chemicals, Ajinomoto Co., Inc.	**Progress in 3D Printed Multi-functional Ceramics** Eric MacDonald, University of Texas, El Paso
4:30pm-5:00pm	**Additive Manufacturing of Micro and Nanoscale Components for Heterogenous Integration and Advanced Packaging** Ahmed Busnaina, Nano OPS, Inc.	**Squaring Off with M-Series Fan-Out Technology** Clifford Sandstrom, Deca Technologies (Benedict San Jose, Deca Technologies; Jen-Kuang Fang, Ping-Feng Yang, Sheng Feng-Huang, Ping-Ching Shen, ASE) Kitabatake, Rintaro Ishii, Katsuyuki Hayashi	**SMART 3D Manufacturing of Printed Electronics** C. Mike Newton, nScrypt/Sciperio (Anand Kulkarni, Kyle Stoodt, Siemens; Emily Sassano, Jason Benoit, Sciperio) Raghunathan, Broadcom

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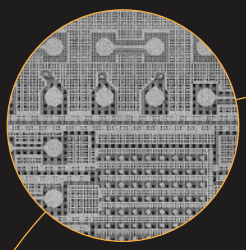
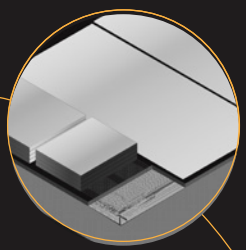
M-Series HD

- Ultra-high-density interconnects
- Multi-mode Adaptive Patterning
- Chiplet integration



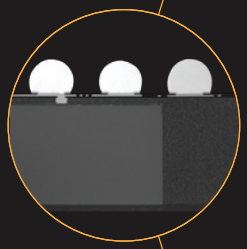
M-Series 3D

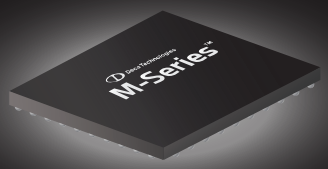
- Chip-first HD
- Chip-last HBM and more
- Embedded 3D interconnects



M-Series CSP

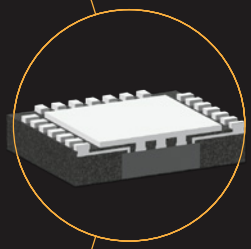
- Fan-in and Fan-out
- Adaptive Alignment™
- Fully encapsulated with superior reliability





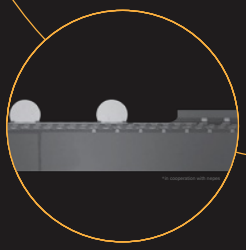
MD-QFN

- Free of leadframe limitations
- Standard and flexible footprints
- 10X scale with 600mm



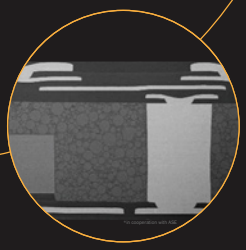
M-Series MCP

- Multi-die
- Adaptive Routing™
- Passive integration



M-Series PoP

- Dual-sided routing
- Dense 3D structure
- Exceptionally thin



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- Die sorting and inspection
- Component inspection and metrology
- IC substrate production processes
- Chemical process control

Device Packaging Technical Sessions - *Tuesday continued*

	HETEROGENEOUS 2D & 3D INTEGRATION Track Wassaja Conference Room 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track Wassaja Conference Room 104-106	NEXT GEN APPLICATIONS Track Wassaja Conference Room 102-103
5:00pm-5:30pm	**Novel IR Laser Debonding for Heterogeneous Integration and 3D Integration** Thomas Uhrmann, EV Group (Peter Urban, Markus Wimplinger, Boris Povazay, Julian Bravin, Bernd Thallner)	**Defluxing of Copper Pillar Bumped Flip Chips** Ravi Parthasarathy, ZESTRON Corporation (Umut Tosun)	**Reliability Investigations in Printed Electronic Assemblies** Beihan Zhao, University of Maryland (Hisham Abusalma, Abhijit Dasgupta, University of Maryland; Edwin Quinn, Laboratory for Physical Sciences; Andres Bujanda, Army Research Lab)
5:30pm-6:00pm	Exhibit Hall Reception Sponsored by: PacTech, JSR Micro, micross		

Tuesday Evening Panel Discussion

6:30pm-8:00pm Wassaja Conference Room 107-108

Sponsored by: evatec, IMAT, TechSearch International

PANEL DISCUSSION on

PACKAGING CHIPLETS: OPPORTUNITIES AND REMAINING CHALLENGES

Moderator:
E. Jan Vardaman, President and Founder, TechSearch International, Inc.

Panelists:
SP Jeng, TSMC
Mike Kelly, Amkor Technology | VP, Advanced Packaging Development and Integration
Choon Lee, JCET Group | Chief Technology Officer
Ravi Mahajan, Intel Corp. | Intel Fellow
Chris Scanlan, Besi Switzerland AG | Senior Vice President Technology

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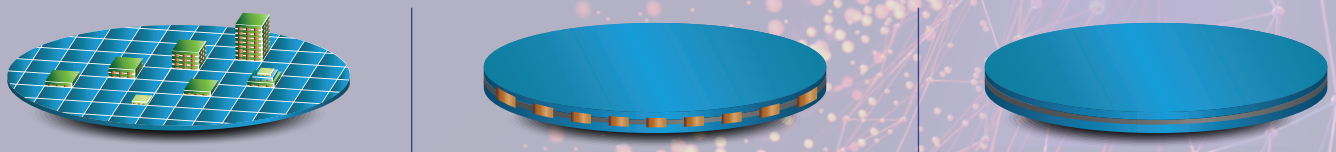
Direct Bonding



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Device Packaging Technical Sessions

Wednesday, March 15

7:00am-6:00pm Registration Wasaja Ballroom Foyer

7:00am-8:00am Continental Breakfast Sponsored by:

GBC Keynote & Plenary Session Wassaja Conference Room 107-108

Sponsored by:

Welcome to the Global Business Council (GBC) Keynote & Plenary Session on

BUILDING THE ECOSYSTEM: TRANSITIONING FROM RESEARCH TO MANUFACTURING

GBC Plenary Session Sponsored by:

8:00am-8:30am	**GBC Opening Comments:** GBC Chair: Lee Smith, Applied Materials
8:30am-9:00am	**Industy Coalition Talk 1 – Advanced Packaging Materials and Open Innovation at Resonac** Hidenori Abe, Resonac
9:00am-9:30am	**Industy Coalition Talk 2 - Glass Core Substrates - Opportunities for CHIPS and MMI** Madhavan Swaminathan, Pennsylvania State University
9:30am-10:00am	**Industy Coalition Talk 3 – New Momentum in Semiconductors: Impact of Ecosystems, a European Case Study** Sylvie Joly, CEA-Leti
10:00am-10:30am	**Networking Break in the Exhibit Hall**
10:30am-10:45am	**Opening -- R&D: The Roots of the Mfg Tree** Moderator: Jan Vardaman, TechSearch International
10:45am-10:55am	Scott Sikorski, ASIC (IBM)
10:55am-11:05am	**Implementation of Applied R&D and European Activities in the Chips Act Age** Peter Ramm, Fraunhofer Research Institution for Microsystems and Solid State Technologies EMFT
11:05am-11:15am	Vic Narusis, Arizona Commerce Authority | Executive Vice President of Business Development
11:15am-12:30pm	**Panel Discussion with the GBC speakers**
10:00am-4:30pm	**Exhibit Hall Open** Wassaja Ballroom

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Device Packaging Technical Sessions - *Wednesday continued*

12:35pm-2:00pm Lunch Break in the Exhibit Hall Sponsored by: ASE

	HETEROGENEOUS 2D & 3D INTEGRATION Track Wassaja Conference Room 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track Wassaja Conference Room 104-106	NEXT GEN APPLICATIONS Track Wassaja Conference Room 102-103
WEDNESDAY AFTERNOON SESSIONS:	**WP1: HYBRID Cu BONDING & MATERIALS** Chairs: Danny Singh, Intel Corp.; Steffen Kröhnert, ESPAT-Consulting	**WP2: FLIP CHIP TECHNOLOGY** Chairs: Danny Brady, Amkor Technology; Knowlton Olmstead, Mercury Systems	**WP3: ADVANCES IN 5G AND MEMS PACKAGING** Chairs: Vidya Jayaram, Intel Corp.; Jaewook Seok, Qualcomm
2:00pm-2:30pm	**D2W Hybrid Bonding using high accuracy carrier solutions for 3D System Integration** Thomas Uhrmann, EV Group (Jürgen Burggraf, Mariana Pires, EV Group; Chun Ho Fan, Hoi Ping Ng, Ming Li, ASMPT)	**Fluxless Thermocompression Bonding of High Density Interconnects Via In-Situ Oxide Reduction as an Alternative to Hybrid Bonding** Bob Chylak, Kulicke & Soffa Industries (Andreas Marte, Horst Clauberg, Tom Colosimo)	**Solutions for Low Cost, Near Hermetic Air Cavity Packages** Don Zyriek, RJR Technologies, Inc.
2:30pm-3:00pm	**High-yield Fabrication of Thin Glass Interposers** Shelby Nelson, Mosaic Microsystems, LLC (David Levy, Kyle Liddle, Patrick Borrelli)	**Advanced IC Substrates for Heterogeneous Integration** Venkata Mokkapati, AT&S (Rozalia Beica)	**RF Packaging and Design for Development of High Performance 5G mmWave Modules** Ivan Ndip, Fraunhofer IZM (Thi Huyen Le, Kavin Murugesan, Uwe Maass, Michael Kaiser, Martin Schneider-Ramelow)
3:00pm-3:30pm	**Chip to Wafer Hybrid Bonding Development for High Volume Manufacturing** Jonathan Abdilla, Besi (Guan Huei See, Raymond Hung, Ruping Wang, Arvind Sundarrajan, Applied Materials; Benedikt Auer, Besi)	**Toward Thinner and Higher Heat Dissipation Advanced Chip Embedded Power Supply Module Packaging** Katsuhiro Takao, AOI Electronics (Atsushi Kuroha, Ichiro Kohno, Takashi Suzuki, Yoshiaki Aizawa)	**Final Finishes for Low Signal Loss: Layer Properties and Reliability of Final Finish Systems Without Nickel** Kuldip Johal, MKS Instruments – MSD, Atotech Deutschland GmbH & Co KG (Britta Schafsteller, Mario Rosin, Dirk Tews, Gustavo Ramos)
3:30pm-4:30pm	**Break in the Exhibit Hall** Wasaja Ballrom		
4:30pm-5:00pm	**3D integration of Detector and ROIC through Wafer Bonding** Iqbal Ali, Cactus Materials, Inc. (Wey Lyn Lee, Brad Lenzen, Rafiqul Islam)	**A Novel 2D/3D X-ray Microscopy Alignment and Inspection Solution for Thermocompression Bonding (TCB) in a Highly Integrated Flip Chip Fan-Out Wafer Level Package (FO-WLP)** Martin Kainz, Besi Austria GmbH (Johannes Ruoff, Holger Blank, Carl Zeiss SMT GmbH; David Taraci, Carl Zeiss Microscopy)	**Glass Package and Through Glass Via (TGV) for MEMS** Aric Shorey, Menlo Microsystems (Chris Keimel)

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Device Packaging Technical Sessions - *Wednesday continued*

	HETEROGENEOUS 2D & 3D INTEGRATION Track Wassaja Conference Room 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track Wassaja Conference Room 104-106	NEXT GEN APPLICATIONS Track Wassaja Conference Room 102-103
5:00pm-5:30pm	**Creating Systems from Chiplets – Next Generation Integration Driven by Hybrid Bonding** Robert Patti, NHanced Semiconductors, Inc.	**Validating Flip Chip Package Models through Experimental Deflection Measurements** Kevin Cox, Tektronix Component Solutions (Jason Krantz, Steven Tonthat, Matt Borden)	**Hermetic Package for MEMS Mirror** Davide Rotta, CamGraPhIC Srl (Marco Chiesa, CamGraPhIC Srl; Marco Del Sarto, Luca Maggi, Amedeo Maierna, STMicrolectronics; Antonella Bogoni, Sant'Anna School of Advanced Studies)
5:30pm-6:00pm	**Hybrid Bond Interconnect for Advanced Packaging Solutions** Thomas Workman, Adeia Inc. (Gill Fountain, Laura Mirkarimi, Guilian Gao, Jeremy Theil, Bongsub Lee)	**Optimizing New Power Switch Technology Using Flip-Chip Assembly** Sam Sadri, QP Technologies (Jiankang Bu, Ideal Power)	**5G mmWave Antenna in Package based on Chip last Fan-out RDL Interposer Technology** Lewis Kang, nepes Corporation

IMAPS POSTER SESSION HAPPY HOUR & 3D InCites DEI FUND NIGHT

Outside on Patio Overlooking Desert (weather permitting)
6:00pm-8:00pm

Session Chairs:
Pui Leng Low, onsemi; Irene Popova, Ancosys, a NOVA Company

Poster Session & Happy Hour Sponsored by:

EMD ELECTRONICS

The Device Packaging Conference Poster Session is not your typical presentation of posters. Set outside with the beautiful view of the mountains, attendees and poster presenters enjoy networking around the fire pits, discussing ideas over a game of cornhole and having a great time with their peers. This is a must attend event!

Device Packaging Technical Sessions - *Wednesday continued*

POSTER SESSIONS

Outside on Patio Overlooking Desert (weather permitting)

Normalized Crack Length - A Means for Evaluating The Relative Risk of BMV Failure
Roger Massey, MKS Atotech (Tobias Bernhard, Kilian Klaeden, Sebastian Zarwell, Edith Steinhaeuser, Sascha Dieter)

Pillars of Wafer Temperature Uniformity and Tuning for sub-10 Reflow Applications
Vladimir Kudriavtsev, Yield Engineering Systems (YES) (Lei Jing, Tapani Laaksonen, Zia Karim, Chris Lane)

Launching the Full Potential of 3D IC with Front-end Architectural Planning
Anthony Mastroianni, Siemens DISW (Gordon Allan)

Winning with 2.5/3D IC Starts with a System-level Golden Netlist
Tarek Ramadan, Siemens DISW (Mike Walsh)

RF Heterogeneous Integration using Photosensitive Glass Ceramics
Jeb Flemming, 3D Glass Solutions, Inc (Kyle McWethy)

From Manhattan to Advanced Package Design
Kyle Fraunfelter, Siemens (Greg Arnot)

Engineered Reliability – Safeguarding Electrical Components and Devices with Nanocoating Technology
Richard Weiland, HZO Inc. (Dan Pulsipher)

MaxQFP TM Exposed Pad (MaxQFP-EP): A Thermally Enhanced MaxQFPTM Platform
Chu-Chung (Stephen) Lee, NXP Semiconductor Inc (Penglin Mei, XS Pang, JZ Yao, Andrew Mawer, Tu-Anh Tran)

The Science Of Adhesion - Insights To Understanding Adhesive Performance
Douglas Katze, Henkel Corp (Yuan-David Zhao, Henkel Corp; Rose Roberts, Brighton Science)

Metal Complex Inks and Films for Additive Manufacturing in Heterogenous Integration and Advanced Packaging Applications
Melbs LeMieux, Sima Hannani, Electroninks

The Grinding and Polishing Technology for Various Materials
Takeru Inoue, Okamoto Corporation

Micro-Textured Film for Immobilizing Bare Die and Packaged Devices During Processing and Handling
Darby Davis, Gel-Pak

Integration of Highly Conductive, Flexible, and Stretchable Interconnects into Li-Metal Battery Packaging
Mayukh Nandy, Siyang Liu, Arizona State University (Yanze Wu, Hongbin Yu)

Macroscopic Stress Quantification of Electrodes in Lithium-Metal Battery Packaging Using Flexible Polymer Current Collector
Mayukh Nandy, Siyang Liu, Arizona State University (Todd Houghton, Hongbin Yu)

Design Optimization and Fabrication of Magnetic Core Inductor in Organic Laminate for Heterogeneous Integration
Mayukh Nandy, Siyang Liu, Arizona State University (Yanze Wu, Hongbin Yu)

UCIe™ (Universal Chiplet Interconnect Express™)
Michael Liu, JCET Group

ALSO IN SESSION WP2: FLIP CHIP TECHNOLOGY

Toward Thinner and Higher Heat Dissipation Advanced Chip Embedded Power Supply Module Packaging
Katsuhiro Takao, AOI Electronics (Atsushi Kuroha, Ichiro Kohno, Takashi Suzuki, Yoshiaki Aizawa)

ALSO IN SESSION TA2: DESIGN & TECHNOLOGY

Cost Analysis of Fan-out Processes for Chiplet Packaging
Amy Lujan, SavanSys Solutions LLC

ALSO IN SESSION THA1: 3D TECHNOLOGY & DESIGN

Incorporating Hierarchical Construction for Advanced IC Packaging
Christopher Cone, Siemens EDA (Edward Hudson)

AWARDS CEREMONY MARCH 14

2023

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Winners announced March 14 @IMAPS DPC after Keynote speakers 9:55am-10:15am

Don't miss the second annual DEI Fund Night and Mural Creation Wednesday, March 15, 6:00-7:15pm

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Thursday, March 16

Arizona Desert Hike

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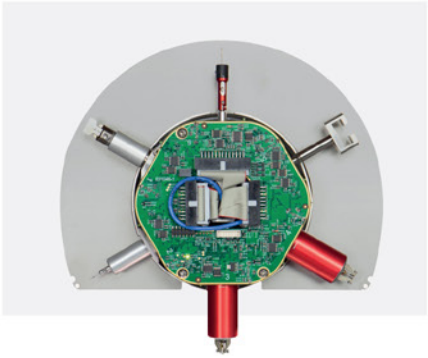


No more cartridge exchanges

Operator free bond testing

High force battery tester

Device Packaging Technical Sessions

Thursday, March 16

7:00am-11:30am Registration Wasaja Ballroom Foyer

7:00am-8:00am Continental Breakfast Sponsored by:

8:00am-8:10am OPENING COMMENTS Wassaja Conference Room 107-108

General Chairs: Nokibul Islam, JCET Group; Scott Hayes, NXP Semiconductors

Plenary/Keynote Sessions Sponsored by:

Thursday, March 16 Keynote Session

8:10am-8:55am

KEYNOTE 3 Wassaja Conference Room 107-108

DRIVING ADOPTION OF ADVANCED IC PACKAGING IN AUTOMOTIVE APPLICATIONS

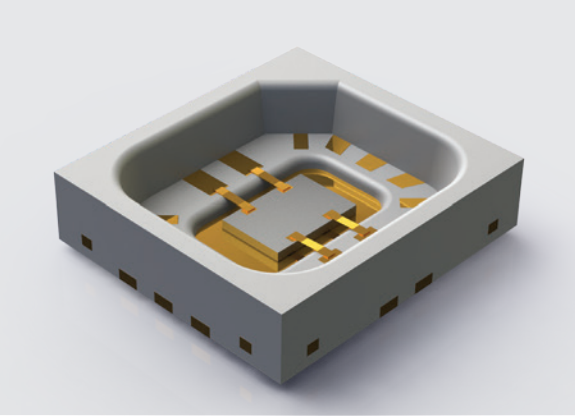
Bassam Ziadeh, General Motors

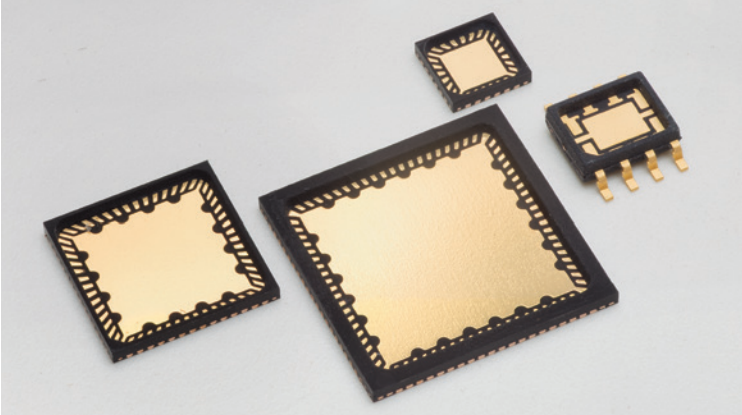
For years automotive semiconductors, have been governed by small, low power Integrated Circuits (ICs) purpose-built for specific functions. These Microcontroller Units (MCUs), deployed on the edge of the computing topology, are typically low-power, low-performance parts. Built on legacy nodes (130nm+) on well-established packaging technology (often wirebond die on QFN-style packages), they demonstrated incremental improvements from a silicon and packaging perspective. With the adoption of software defined vehicles (SDV), the evolution of advanced driver assist systems (ADAS), and feature rich in-vehicle infotainment (IVI), the per vehicle computer power has grown exponentially per vehicle, colloquially, known as data centers on wheels. With this growth has come the need to adopt newer packaging techniques to improve system latency, bandwidth, computer power, and IP integration and reducing the system footprint via 3D stacking – all fabricated on leading edge nodes.

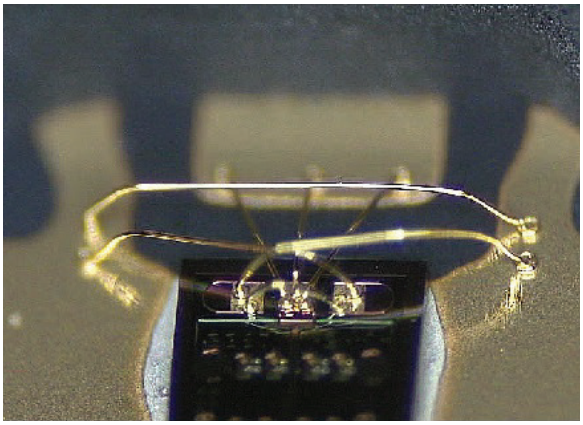
Advanced packaging has seen tremendous growth and adoption in the data center and client ecosystems – the next hurdle is addressing the safety and reliability focused requirements of automotives; extended useful lifespan of 10yrs+, and weathering harsher environmental conditions of thermal extremes, vibration, EMC, and mixed IP integration. This talk will address the areas of focus for adopting heterogenous integration and advanced automotive packaging for automotives such as qualification and formulation of materials to minimize traditional packaging yield concerns, introduction of new thermal interface materials aligned with new liquid cooled ECUs and testing to ensure zero defects across chiplets and memory; with broader test coverage and the adoption of Known Good Die (KGD). Additionally, the talk will cover the importance of driving industry standardization regarding die-to-die communication protocols, form factors, power delivery, system integration, and qualifying/enveloping new failure modes from the current baseline AEC-Q100 requirements brought on by various 2.5D and 3D packaging.

Bassam Ziadeh *is a Global Technical Specialist at General Motors responsible for advanced package architecture roadmap and strategy definition. He was a technologist at Intel for 11 years working on inventing and developing novel technologies and architectures for advanced packaging prior to moving to General Motors to put these technologies into action and drive broader industry adoption. He received his Bachelors from the University of Jordan in 2010 and Masters from Arizona State University in 2011. He has over 15 US and International patents in the field of packaging and process technology and is a member of the UCIe Consortium.*

RF applications (5G), MEMS, sensors and power semiconductors command specialty packages







- OmPP air-cavity QFN, standard JEDEC configurations available off the shelf
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Device Packaging Technical Sessions - *Thursday continued*

Thursday, March 16 Keynote Session	
8:55am-9:40am	**EXTENDING MOORE'S LAW WITH INTEGRATED PHOTONICS** Wassaja Conference Room 107-108  **Nicholas Harris, Lightmatter** The insatiable growth in computing needs, coupled with the end of Denard Scaling and the slowdown of Moore's Law, is resulting in a major shift across the industry towards a chiplets-based product architecture. Solutions that enable the heterogeneous integration of disaggregated silicon at high data rates and low power are becoming increasingly important. Silicon photonics-based interconnect solutions play a critical role in enabling this integration. *Harris has over 30 patents and 70 publications in journals including Nature, Nature Photonics, and Nature Physics.* **Nicholas Harris'** *work on quantum and classical information processing with integrated photonics has helped launch the international research field of programmable photonics. Nicholas has been recognized by the MIT Technology Review through the prestigious Innovators Under 35 Award. He received his doctorate in Electrical Engineering and Computer Science at the Massachusetts Institute of Technology where he was a National Science Foundation Graduate Research Fellow and later worked as a Postdoctoral Fellow through the Intelligence Community Postdoctoral Fellowship.*
9:40am-10:00am	**Break in Foyer**

Device Packaging Technical Sessions - *Thursday continued*

	HETEROGENEOUS 2D & 3D INTEGRATION Track Wassaja Conference Room 107-108	FAN-OUT, WAFER LEVEL PACKAGING & FLIP CHIP Track Wassaja Conference Room 104-106	NEXT GEN APPLICATIONS Track Wassaja Conference Room 102-103
THURSDAY MORNING SESSIONS:	**THA1: 3D TECHNOLOGY & DESIGN** Chairs: Sanketh Buggaveeti, Infinera; Hongbin Yu, Arizona State University	**THA2: SUBSTRATE TECHNOLOGY** Chairs: Christo Bojkov, Qorvo ; Mark Kuhlman, Qualcomm	**THA3: IMPROVING RELIABILITY IN ELECTRONICS** Chairs: Brian Lynch, MacDermid Alpha Electronics Solutions; Ao Wang, Intel Corp.
10:00am-10:30am	**The Evolution of Moore's Law through Chipletized Architectures** Victor Medrano, Tony Trinh, Mercury Systems (Tom Smelker)	**High Speed Acid Copper Plating for IC Substrates** Sean Fleuriel, MacDermid Alpha Electronics Solutions (Kesheng Feng, Confesol Rodriguez, MacDermid Alpha Electronics Solutions; Robert Moon, Delores Cruz, Jonathan Hander, ASMPT-NEXX)	**Warpage and Reliability Study of Large Size XDFOI™ FO-MCM fcBGA** Danfeng Yang, JCET Group (Allen Xu, Nokibul Islam, Coco Xu, Yaojian Lin)
10:30am-11:00am	**AI, ML and DL Applications for Semiconductor Package Design and Verification** John Ferguson, Siemens DISW (Per Viklund)	**Low Loss/Low Modulus/Low CTE Semiconductor Carrier Packaging Thin Core Substrate Material** Caleb Ancharski, AGC Multi Material America (Thomas McCarthy, Preeya Kuray, Mark Derwin)	**Processing and Reliability Testing of a Copper Pressure Sinter Paste for use in High Power Module, Die Attach applications** Dean Payne, Indium Corporation (Min Yao, Hongyun Li)
11:00am-11:30am	**Enabling Co-Design for 3D Heterogenous Integrated Packages** John Park, Cadence Design Systems	**Advanced IC Substrate Deformation and Pattern Distortion Analysis to Validate the Use of an Extremely Large Exposure Field Fine-Resolution Lithography Solution** Keith Best, John Chang, Onto Innovation (Corey Shay, James Webb, Timothy Chang)	**Cu Wirebond Technology in 16FFC High Performance Automotive Radar Processor with IR Drop Reduction Methodology** Tu-Anh Tran, NXP Semiconductor (Jasmine Lim, Y.K. Au, M.J. Song, Mollie Benson)
11:30am-12:00pm	**Incorporating Hierarchical Construction for Advanced IC Packaging** Christopher Cone, Siemens EDA (Edward Hudson)	**Advanced Glass Carriers for Buildup Structure Warp Control and Wafer Ultra-thinning** Jay Zhang, Corning Inc. (Andy Teng, Christina Yu)	**OSAT Production Testing of 5G, Power Discretes & 3D packaged ICs** Vineet Pancholi, Amkor Technology
12:00pm	**Conference Ends**		

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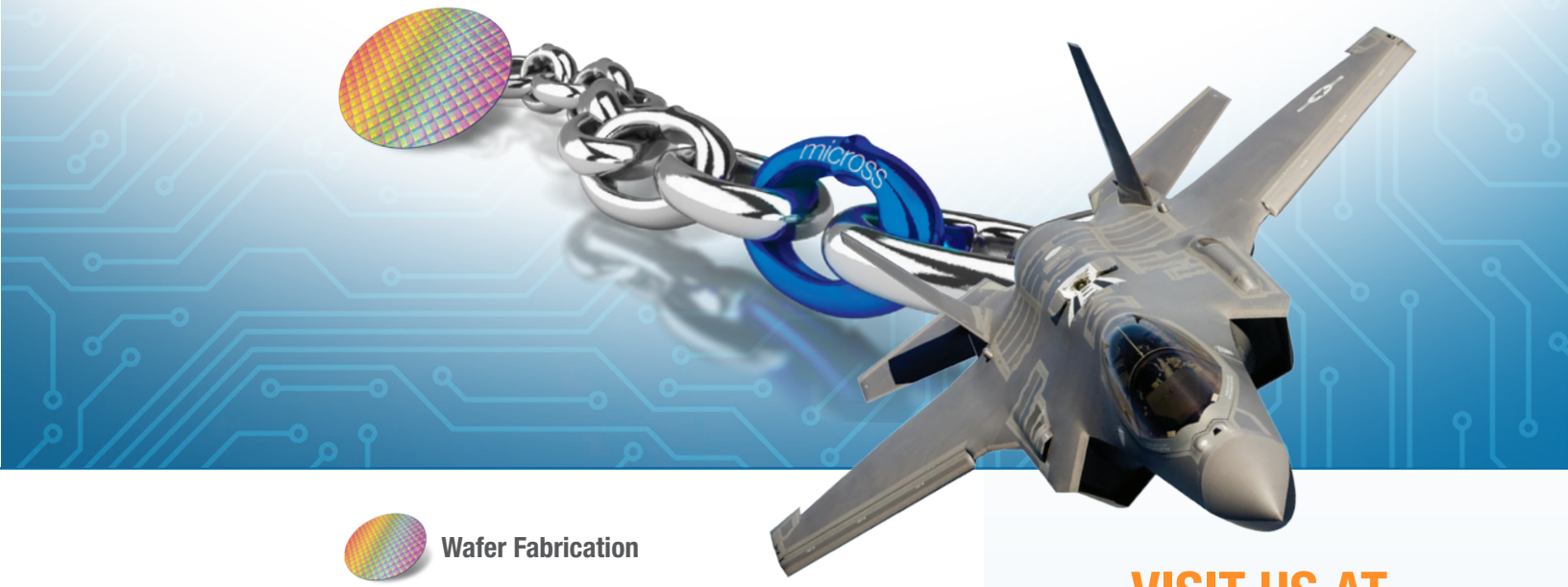

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Micross will be showcasing our latest solutions for the aerospace, defense, and other hi-rel markets. Our product experts and executives will be on site to discuss your technical and program needs. Scan the QR code to schedule a meeting today!

Post-Conference Fundraising Events

2023 David Virissimo Spring Charity Golf Outing

benefiting the

Microelectronics Foundation

Thursday, March 16, 2023

4-Person Scramble | 1:00 PM Shotgun Start

Check-in: 12:00-1:00 PM

SunRidge Canyon Golf Club
13100 N Sunridge Dr., Fountain Hills, AZ
http://www.sunridgegolf.com/

Rental Clubs are paid directly to the Clubhouse – Call 480-837-5100

Cost: $235 per golfer or $950 for foursome

The cost includes: Transportation to and from the course, greens/cart fees, shotgun start, and awards reception/dinner following your round. All proceeds from this event will benefit the IMAPS Microelectronics Foundation.

Click here for complete information.

3DInCites Hike For DEI

Sponsored by KLA

If you're not participating in the golf tournament, why not join us for a guided, afternoon hike in the nearby McDowell Sonoran Preserve?

All proceeds benefit the 3D InCites DEI Fund, established to help tech start-ups owned by women and under-represented minorities grow and thrive.

When:
Thursday, March 16
from 12:30pm-4pm

Cost: **$75**
(includes transportation from We-ko-Pa Resort)

Get Registered to Hike!

The hike can be added during the conference registration process by selecting hike options on the second page of registration fees (an "add on" to your conference selection).

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Extending our global production footprint and boosting R&D and innovation.

In May 2023, we will inaugurate a new factory in Chandler, AZ for the manufacture of equipment for our Delivery Systems & Services (DS&S) business which will contribute to the growth of the local semiconductor industry.

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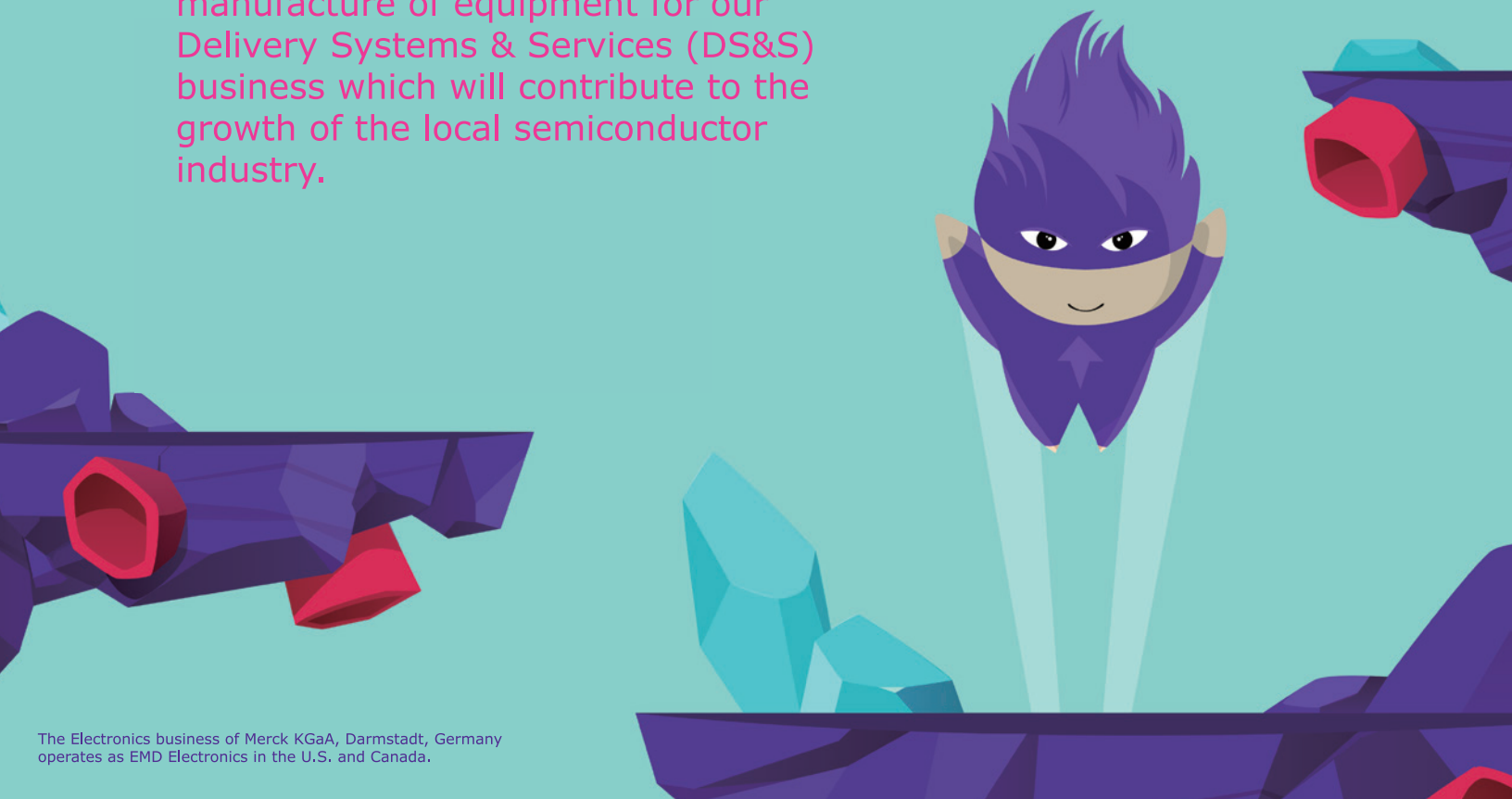

Exhibit Hall Floorplan

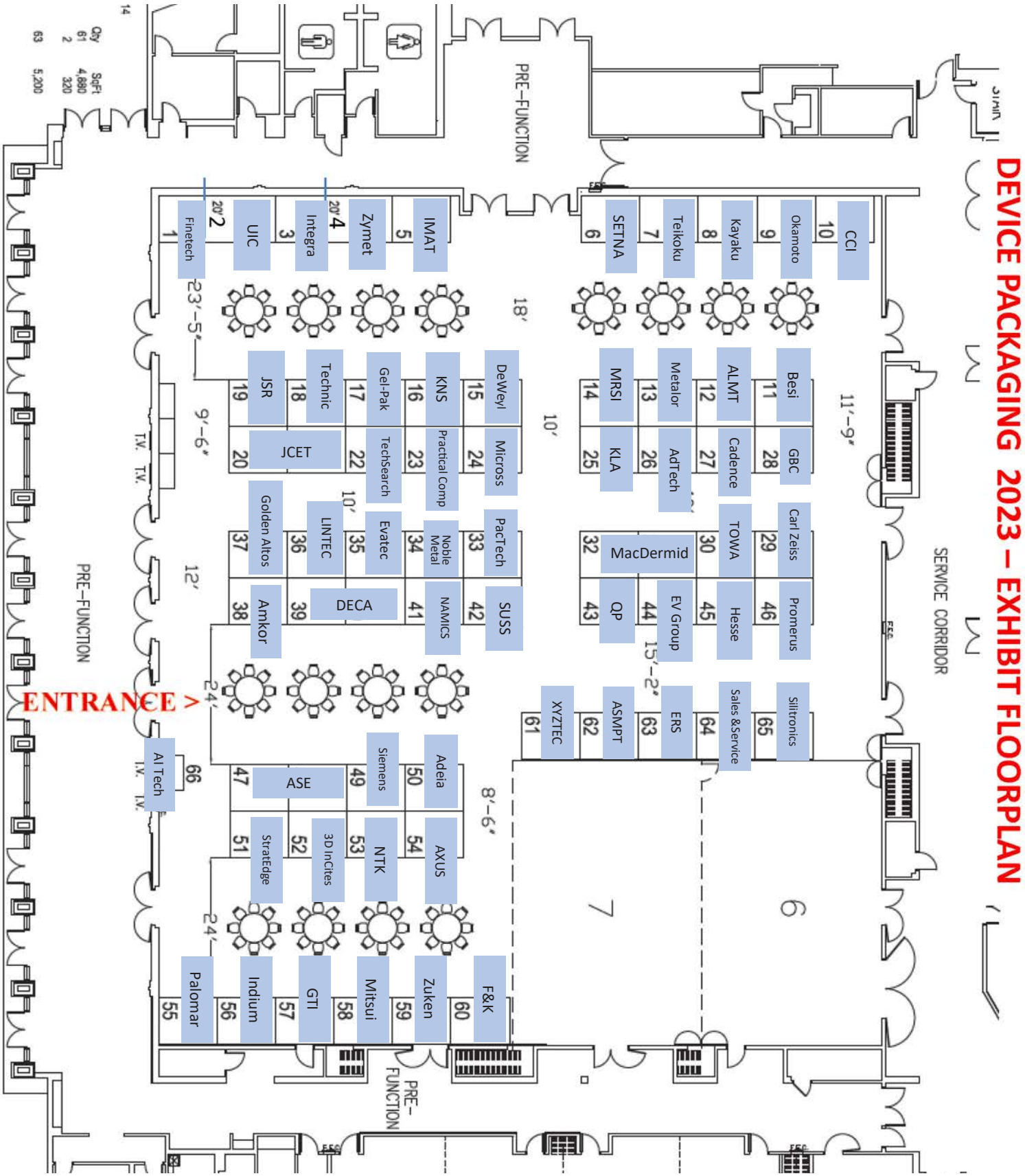

Exhibit Booth Numbers

Booth#	Exhibitor
52	3DIncites
50	Adeia (XPERI)
26	AdTech Ceramics
66	AI Technology Inc.
12	ALMT Corp./Sumitomo Electric USA
38	Amkor Technology, Inc.
47/48	ASE Group
62	ASMPT Semiconductor Solutions
54	Axus Technology
11	Besi North America, Inc.
27	Cadence
29	Carl Zeiss Microscopy
10	Conductive Containers, Inc.
39/40	Deca Technologies Inc.
15	DeWeyl Tool Company
63	ERS Electronic GmbH
44	EV Group
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60	F&K Delvotec, Inc.
1	Finetech USA
28	GBC Advanced Materials LLC
17	Gel-Pak
37	Golden Altos Corp
57	GTI Technologies, Inc.
45	Hesse Mechatronics, Inc.
5	IMAT Inc.
56	Indium Corp.
3	Integra Technologies
20/21	JCET Group
19	JSR Micro
8	Kayaku Advanced Materials
25	KLA
16	Kulicke & Soffa Industries

Booth#	Exhibitor
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31/32	MacDermid Alpha Electronics Solutions
13	Metalor Technologies USA
24	Micross Components
58	Mitsui Chemical America
14	MRSI Systems, Mycronic Group
41	NAMICS Technologies, Inc.
34	Noble Metal Services
53	NTK Technologies
9	Okamoto Corporation
33	PacTech USA Packaging Technologies, Inc.
55	Palomar Technologies Inc.
23	Practical Components
46	Promerus LLC
43	QP Technologies
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65	Silitronics
51	StratEdge Corp
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18	Technic
22	TechSearch International, Inc.
7	Teikoku Taping System, Inc.
30	TOWA USA Corporation
2	Universal Instruments
61	XYZTEC, Inc.
59	Zuken, Inc.
4	Zymet, Inc.

2023 Exhibitor Directory

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Booth: 52
3DIncites
Phoenix, AZ
www.3dincites.com

The 3D InCites Community was established in 2009 to stir up interest in 3D integration. Now in its 14th year, 3D InCites has broadened its scope stir up interest in heterogeneous integration. As such, 3D InCites is about much more than just through-silicon vias and subsequent stacking technologies. Rather, 3D InCites has become part of the whole advanced packaging conversation as it relates to heterogeneous integration, the internet of things, and other applications these technologies enable. The goal is to inform key decision-makers about progress in technology development, design, standards, infrastructure, and implementation. As a community, 3D InCites brings to life the people, the personalities, and the minds behind heterogeneous integration and related technologies in a uniquely personal way. As the interests and concerns of our community expand, so do our areas of coverage. That's why in 2021, we added efforts to build awareness around the importance of sustainable semiconductor manufacturing, and diversity equity and inclusion in the workplace. Our goal is to support the efforts of our community members.

Booth: 12
A.L.M.T. Corp.
Chuo-ku, Tokyo, JAPAN
https://www.allied-material.co.jp/en.html

Taking advantages of materials such as tungsten, molybdenum, and diamond, we manufactures high quality heatspreader materials. Applications of these materials include electronics, automotive, aerospace, and many more.

Booth: 50
Adeia
San Jose, CA
www.adeia.com

Adeia invents, develops and licenses fundamental innovations that shape the way millions of people explore and experience entertainment and enhance billions of devices in an increasingly connected world. Leveraging the combination of highly experienced technologists, scientists, engineers and advanced R&D labs in San Jose, California and Raleigh, North Carolina, Adeia develops industry-leading 3D integration solutions such as hybrid bonding that meet the demand for greater functionality, higher performance and smaller size for next generation electronics. For more information, please visit adeia.com.

Booth: 26
AdTech Ceramics Co.
Chattanooga, TN
www.adtechceramics.com

AdTech Ceramics is a certified manufacturer of custom hermetic ceramic and metal packages that are used with active & passive electronic components. Ceramic materials include alumina 92% (HTCC) and Aluminum nitride (AIN). Core competencies include custom design support, tape casting, multilayer ceramic processing, brazed assemblies, plating, metal/ceramic packaging, & chemical milling. Chemical milling of alloy 42 and Kovar includes leads, stepped lids, seal rings and filters all made to custom requirements. Engineering support is available for package design from initial concepts to prototypes, to full production. Primary markets served are medical, military, and high reliability industrial applications. Manufacturing capability includes prototype to high volume production. US based company is ISO 9001:2000 certified, DFARS 252-225-7014 Alt compliant

Booth: 66
AI Technology Inc.
Princeton Junction, NJ
www.aitechnology.com

AI Technology, Inc. (AIT) developed Flexible Epoxies for Microelectronic packaging in 1985. AIT specializes in Electronic Interconnect and Microelectronic packaging materials, offering Molecularly Flexible Epoxy Adhesives for Die-Attach, Substrate Attach or Permanent Bonding, Adhesives and Underfills for multi-size Die bonding, Die Attach Film (DAF) for stack-chip packaging, Flip-Chip bonding, and underfilling, High Temperature single and multi-chip module die bonding over 230°C. Component and Substrate bonding adhesives for Military and Commercial applications.

AIT's Thermal Interface Materials, including Phase-change pads, Greases, Gels, and Adhesives, ensure ultimate performance and heat dissipation in Semiconductors, Modules, Computers, and Electronic Communication applications.

Our Wafer Processing Adhesive (WPA), is a temporary film format high-temperature bonding adhesive for thin wafer processing of bonding device wafer to a carrier wafer. Additionally, Other products include Conformal Coatings and Protective Coatings for ultimate moisture and/or humidity protection as well as UV resistance.

2023 Exhibitor Directory

Booth: 38
Amkor Technology, Inc.
Tempe, AZ
www.amkor.com

Amkor Technology is one of the world's largest providers of high-quality semiconductor packaging and test services. Founded in 1968, Amkor pioneered the outsourcing of IC packaging and test and is a strategic manufacturing partner for the world's leading semiconductor companies, foundries and electronics OEMs.

Amkor's broad package portfolio and technology leadership offer our customers semiconductor and test solutions to enable 5G, AI, Automotive, Communications, Computing, Consumer, Industrial, IoT and Networking products.

Services include package design and development, wafer probe and package test, wafer bumping and redistribution, package assembly and final test. Engineering services offer best-in-class thermal, electrical and mechanical modeling and characterization as well as design automation. Test engineering services range from test program development to full product characterization of packaged RF, mixed signal, logic and memory devices.

Amkor offers a flexible supply chain including production facilities, product development centers and sales and support offices located in key electronics manufacturing regions in Asia, Europe and the US. For more information, visit www.amkor.com.

2023 Exhibitor Directory

Booth: 47-48
ASE, Inc.
Sunnyvale, CA
www.aseglobal.com
ASE, Inc. is the leading global provider of semiconductor manufacturing services in assembly and test. In a world running on semiconductor technology to achieve lifestyle, efficiency and sustainability goals, packaging innovation is at the heart of what ASE does. ASE today is delivering on the promise of heterogeneous integration, through advanced packaging, system-in-package, and chiplet solutions to meet growth momentum across HPC, Automotive, AI, 5G, and more. To learn about our technology advances and our VIPack™ platform, designed to enable vertically integrated package solutions, please ask the ASE experts at our IMAPS booth or visit aseglobal.com or follow us on Linkedin: @aseglobal.

Booth: 62
ASMPT SEMI USA, Inc.
Tempe, AZ
https://www.asmpt.com/
Globally headquartered in Singapore, ASMPT is a leading global supplier of hardware and software solutions for the manufacture of semiconductors and electronics, with a truly unique, broad-based portfolio that sets us apart from others. ASMPT's solutions range from wafer deposition and laser grooving to the others that shape, assemble and package delicate electronic and optical components into a vast range of end-user devices, which include electronics, mobile communications, computing, automotive, industrial and LED (displays). ASMPT's continuous investment in R&D also helps provide cost-effective, industry-shaping solutions that address customers' critical requirements and help shape a bright & sustainable future.

Booth: 54
Axus Technology
Chandler, AZ
https://axustech.com/
Axus Technology is a global OEM company based in Chandler, Arizona, bringing the latest surface processing solutions to emerging technology industries such as Semiconductor, MEMS, Automotive, Defense and Aerospace, Lifesciences, and IoT. We provide advanced CMP tools and technology, along with exceptional technical expertise for polishing, wafer cleaning, and precision wafer grind processing; making us one of the best highly specialized technology suppliers and consulting services focused on engineering capability and efficiency in supporting the CMP market. With a fully equipped class 100 foundry cleanroom, Axus Technology can help facilitate your need for advances in wafer technology and efficient wafer production with new designs and novel applications. We implement turnkey solutions for process development, foundry processing, and equipment tooling including tool installation and training, field service, and consumable selection.

Booth: 11
Besi North America, Inc
Chandler, AZ,
www.besi.com
Besi is a leading supplier of assembly equipment for the global semiconductor and electronics industries offering high levels of accuracy, productivity and reliability at a low cost of ownership. Besi has developed leading edge assembly processes ranging from advanced Hybrid Bonding with sub-micron accuracy to equipment for leadframe, substrate and wafer level packaging applications. Besi's equipment offerings include conventional and advanced die attach, molding, trim & form, saw singulation and plating. Besi supports a wide range of end-user markets including electronics, mobile internet, computer, automotive, industrial, LED and solar energy. Besi customers are primarily leading semiconductor manufacturers, assembly subcontractors and electronics and industrial companies. The principal brand names for Besi's assembly equipment systems include Datacon, Esec, Fico and Meco.

Booth: 27
Cadence Design Systems
San Jose, CA
www.cadence.com
Cadence is a pivotal leader in electronic design, building upon more than 30 years of computational software expertise. We apply our underlying Intelligent System Design strategy to deliver software, hardware, and IP that turn design concepts into reality. Our customers are the world's most innovative companies, delivering extraordinary electronic products from chips to boards to systems for the most dynamic market applications, including consumer, hyperscale computing, 5G communications, automotive, mobile, aerospace, industrial, and healthcare. Seven years in a row, Fortune magazine has named Cadence one of the 100 Best Companies to Work For. Learn more at www.cadence.com

Booth: 29
Carl Zeiss Microscopy, LLC
White Plains, NY
www.zeiss.com/microscopy
ZEISS has the most comprehensive portfolio of light, X-ray and electron/ion beam imaging technologies in the industry. Solutions span from wafer fab through packaging and assembly. ZEISS materials characterization and non-destructive FA solutions deliver actionable information to meet industry challenges for next-generation devices

Booth: 10
Conductive Containers, Inc
New Hope, MN
www.corstat.com
Conductive Containers, Inc. (CCI) is the industry leader in ESD safe material handling and packaging. Our capabilities include Thermoforming and injection molding of plastics, Corstat and Conductive Fluted Plastic boxes, KleanStat Flex and foam converting.

2023 Exhibitor Directory

Booth: 39-40
Deca
Tempe, Arizona
www.thinkdeca.com

Deca was born of a passion to transform the way the world builds advanced electronic devices. In our first decade, our 10X thinking brought to life exciting breakthroughs with M-Series™ and Adaptive Patterning®. Our flagship M-Series is a fully encapsulated wafer & panel-level fan-out technology which provides an ideal structure for single & multi-die packaging, chiplet integration, 3D PoP and embedded die interposers. M-Series is delivering exceptional quality and reliability for leading Smartphone manufacturers around the globe with shipment volumes exceeding one billion units per year. Deca's Adaptive Patterning technology compensates for natural variation in embedded die structures without costly processes or design limitations. After high-speed optical measurement, Adaptive Patterning generates a bespoke and optimized layout which is precisely aligned to each device. The power of Adaptive Patterning is realized through Adaptive Patterning Design Kits (APDKs) with provide integrated design templates, tech files, stack-ups, DRC decks, and AP Studio software. As a pure-play technology development, transfer and licensing company, Deca is the leading independent provider of advanced packaging technology in the semiconductor industry. Our world class investors, including Infineon, Qualcomm, ASE, nepes and SunPower provide Deca with a strong foundation for continuing innovation and growth. Contact us at ThinkDeca.com

2023 Exhibitor Directory

Booth: 15
DeWeyl Tool Company
Petaluma, CA
www.deweyl.com

DeWeyl provides the finest quality bonding wedges in the world. Located in the Petaluma, CA, DeWeyl's primary business is manufacturing wire bond wedges and custom high precision tooling for the semiconductor, aerospace and medical industry. DeWeyl produces wedges made from ceramic, titanium and tungsten carbide for small and large round wire and ribbon applications.

Booth: 63
ERS Electronic GmbH
Germering, Germany
www.ers-gmbh.de

ERS electronic GmbH, based in Germering close to Munich, has been providing innovative thermal management solutions to the semiconductor industry for more than 50 years. The company has gained an outstanding reputation, notably with its fast and accurate air cooling-based thermal chuck systems for test temperatures ranging from -65°C to +550°C for analytical, parameter-related and manufacturing probing.

ERS also supplies the Advanced Packaging market with its fully automatic and manual debonding and warpage adjust tools used for Fan-Out Wafer-Level-Packaging (FOWLP) and Panel-Level-Packaging (FOPLP) technologies up to 650 x 650 mm format.

Our headquarter, sales department, engineering center and production facilities are in the Munich suburb of Germering, and we also have sales and support offices worldwide.

Booth: 44
EV Group, Inc.
Tempe, AZ
https://www.evgroup.com/

EV Group (EVG) is a leading supplier of high-volume production equipment and process solutions for the manufacture of semiconductors, MEMS, compound semiconductors, power devices and nanotechnology devices. A recognized market and technology leader in wafer-level bonding and lithography for advanced packaging and nanotechnology, EVG's key products include wafer bonding, thin-wafer processing and lithography/ nanoimprint lithography (NIL) equipment, photoresist coaters, as well as cleaning and inspection/metrology systems. With state-of-the-art application labs and cleanrooms at its headquarters in Austria, as well as in North America and Asia, EVG is focused on delivering superior process expertise to its global R&D and production customer and partner base – from the initial development through to the final integration at the customer's site. Founded in 1980, EVG services and supports an elaborate network of global customers and partners all over the world, with more than 1200 employees worldwide and fully-owned subsidiaries in the U.S., Japan, South Korea, China and Taiwan.

Booth: 35
Evatec NA Inc
San Jose, CA
www.evatecnet.com

Evatec provides PVD solutions tailored to the packaging platforms in the Advanced Packaging market. They combine best in class cost of ownership with unique technology innovations to meet today's and future requirements. Our "wafer" platforms process up to 300mm formats designed for highest levels of throughput, support the use of long life targets and are equipped with a unique degassing technology that achieves best in class contact resistance and layer uniformity performance required in WLCSP, FOWLP and 2.5D/3D devices. FOPLP applications and next generation IC substrate technologies are supported by Evatec`s CLUSTERLINE® 600 equipment platforms capable of processing substrate sizes up to 650 x 650 mm, deliver highest levels in outgassing performance, layer adhesion and stack uniformity. In EMI shielding of chips on a package level, Evatec offers production solutions with the step coverage, film adhesion and low process temperatures required to protect the chip effectively at high throughput.

Booth: 60
F&K Delvotec
Foothill Ranch, CA
www.fkdelvotec.com

F & K DELVOTEC was founded in 1978 and has produced revolutionary new technologies that have subsequently progressed to market standards. Our State-of-the-art M17S wire bonder could be used for all wire bond processes (Ball-wedge, wedge-wedge for thin and heavy wire/ribbon). Our new M17LSB laser bonding equipment is the ideal solution for metal to metal interconnections. For consultation, product inquiries, pre-production support, and further information please feel free to contact us at 949-595-2200.

Booth: 1
Finetech USA
Amherst, NH
www.finetechusa.com

Finetech offers precision die bonders for advanced packaging -- flip chip, VCSELs, laser bars & diodes, sensors, photonics packaging, MEMs, C2W, Cu pillar, and Chip on Glass. A high degree of process flexibility makes these systems ideal for R&D or prototype -- thermo-compression, thermo-sonic, eutectic, epoxy, ACF & Indium bonding. Manual and automated models available, with sub-micron placement accuracy. Engineering collaboration for complex and novel applications.

2023 Exhibitor Directory

Booth: 28
GBC Advanced Materials LLC
Latrobe, PA 15650
www.gbcmaterials.com
GBC Advanced Materials LLC offers Precision Manufacturing of Glass, and Ceramic Components for the Electronic Packaging, Medical Devices, and Aerospace components. GBC can Mechanical Press Ceramic and Glass Powders as well as machine parts in the Green State, fire to size and ship, which results in short lead time for our customers.

Booth: 17
Gel-Pak
Hayward, CA
www.gelpak.com
At Gel-Pak, we develop and manufacture a family of polymer-based carriers and films designed to provide maximum protection during the shipping, handling and processing of delicate devices. Our manufacturing expertise allows us to customize existing products or rapidly develop novel solutions to meet evolving requirements for demanding environments. Headquartered in Hayward, California, we have manufacturing device carriers since 1980.

Booth: 37
Golden Altos Corp.
Milpitas, CA
www.goldenaltos.com
Golden Altos is a QML provider of assembly services (http://www.goldenaltos.com) and we are located in the heart of the silicon valley (Milpitas, CA). Golden Altos offers complete on-shore, in-house, high-reliability hermetic assembly for both monolithic and hybrid assemblies as well as qualification services for both hermetic and plastic IC's. We continually strive to deliver the finest products, services and documentation through our own internal system, as well as regular certifications from government agencies. As a small business that has served the commercial, military, and aerospace industries for over 30 years, Golden Altos understands the importance of putting our customers first because what we do matters.

Booth: 57
GTI Technologies, Inc.
Shelton, CT
https://gti-usa.com/
GTI Technologies is a full-service distributor and importer of high precision manufacturing equipment for the semiconductor, advanced materials, and metalworking industries. Founded in October 1978 as Grinding Technology Inc., GTI Technologies began as a representative organization providing sales and service for number of precision European grinding machine manufacturers throughout North America. In the beginning, our customer base consisted of traditional automotive, aerospace and general manufacturing customers. Shortly thereafter, we began working with GMN, and Bell Lab's engineers to develop the first silicon wafer backside grinders for the fledgling semiconductor industry. The emergence of the semiconductor and electronics industries opened new doors of opportunity for GTI. We soon added new lines to our semiconductor products including Takatori Corporation, who was an industry leader in automated tape /de-tape systems to support the back grinding process. Over the years, GTI has gradually transitioned its business to focus primarily on the semiconductor industry. With this transition our base of operations has been expanded to include Europe. Since GTI's founding in 1978, we have been on the leading edge of our specialties. We bring over 40 years of experience to the products we offer and aftermarket support that is second to none.

Booth: 45
Hesse Mechatronics
San Jose, CA
www.hesse-mechatronics.com
Hesse Mechatronics, Inc. (formerly Hesse & Knipps, Inc.) is the Americas subsidiary of Hesse GmbH, world leader in wedge wire bonding technology for backend semiconductor assembly in the power, automotive, medical, aerospace, RF, microwave, opto, military and consumer electronics industries. The company designs and manufactures high speed, fully automatic fine pitch thin wire bonders for aluminum and gold round wire and ribbon, and heavy wire bonders for aluminum, gold and copper round wire and ribbon, including HCR™ (High Current Ribbon). The company's product line also includes dispensers, ultrasonic flip chip bonders, standard or customized indexers with or without handling systems, manufacturing process monitoring systems for interfacing with the company's equipment and commercial software packages. In addition to the most advanced wire bonding equipment, Hesse Mecharonics, Inc. also provides wire bonding equipment training, applications support, development and production of wire bonding prototypes and pre-production manufacturing in four applications and demonstration labs throughout the USA.

2023 Exhibitor Directory

Booth: 5
IMAT Inc.
Clinton, MA
www.imatinc.com
We offer a full suite of processing from metal deposition, thermal oxide and photolithography services. Contact us today for your custom processing needs.

Booth: 56
Indium Corporation
Clinton, NY
www.indium.com
Indium Corporation® is a premier materials refiner, smelter, manufacturer, and supplier to the global electronics, semiconductor, thin-film, and thermal management markets.

Booth: 3
Integra Technologies Inc
Wichita, KS
www.integra-tech.com
Integra Technologies is a global leader in the sourcing, packaging, testing and characterization of highly specialized, mission-critical semiconductor components and related value-added services for high-reliability ("Hi-Rel") applications where dependability and failure-free performance are of paramount importance. Integra provides a span of in-house services and capabilities to support a broad variety of Hi-Rel components throughout the entire value-added life-cycle - from prototyping, through testing, and ultimately to volume production. More specifically, Integra specializes in semiconductor die prep, packaging, assembly, test, reliability qualification, DPA and FA service for high-reliability applications

Booth: 20-21
JCET
Milpitas, CA
www.jcetglobal.com
JCET Group is the world's leading integrated-circuit manufacturing and technology services provider, offering a full range of turnkey services that include semiconductor package integration design and characterization, R&D, wafer probe, wafer bumping, package assembly, final test and drop shipment to vendors around the world. Our comprehensive portfolio covers a wide spectrum of semiconductor applications such as mobile, communication, compute, consumer, automotive, and industrial, through advanced wafer-level packaging, 2.5D/3D, System-in-Package, and reliable flip chip and wire bonding technologies. JCET Group has two R&D centers in China and Korea, six manufacturing locations in China, Korea, and Singapore, and sales centers around the world, providing close technology collaboration and efficient supply-chain manufacturing to our global customers.

Booth: 19
JSR Micro, Inc.
Sunnyvale, CA
https://www.jsrmicro.com
JSR's THB series of thick film photoresists, along with WPR series of dielectric coatings and LP series of lift-off photoresists, offer advanced packaging technology portfolios to enable manufacturing of WL-CSP, Flip Chip, TSV, LED and MEMS devices with fine-pitched and cost effective micro-bump, Cu-pillar, RDL, and lift-off processes.

Booth: 8
Kayaku Advanced Materials
Westborough, MA
www.kayakuAM.com
Kayaku Advanced Materials, Inc., a wholly owned subsidiary of Nippon Kayaku Co. Ltd., is a manufacturer of specialty electronic materials, providing innovative chemical solutions to MEMS, microelectronic and semiconductor markets. It specializes in photoimageable epoxy; e-beam, bi-layer lift-off & dielectric resists; and a suite of ancillary lithography products, as well as plating & RDL materials for advanced packaging. Additionally, Kayaku Advanced Materials' product lines include PriElex functional printed electronic inks & coatings; and Paratronix parylene & SignalSeal conformal coating services & equipment sales. Kayaku Advanced Materials also has an exclusive licensing and distribution partnership with DuPont Electronic Materials for DuPont semiconductor & advanced packaging electronic materials.

Booth: 25
KLA Corporation
Milpitas, CA
https://www.kla.com/
KLA develops industry-leading equipment and services that enable innovation throughout the electronics industry. We provide advanced process control and process-enabling solutions for manufacturing wafers and reticles, integrated circuits, packaging, printed circuit boards and flat panel displays. In close collaboration with leading customers across the globe, our expert teams of physicists, engineers, data scientists and problem-solvers design solutions that move the world forward.

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eda.sw.siemens.com/en-US/ic-packaging

2023 Exhibitor Directory

Booth: 16
Kulicke & Soffa Industries Inc.
Fort Washington, PA
www.kns.com
Kulicke & Soffa (NASDAQ: KLIC) is a leading provider of semiconductor, LED and electronic assembly solutions serving the global automotive, consumer, communications, computing and industrial markets. Founded in 1951, K&S prides itself on establishing foundations for technological advancement - creating pioneering interconnect solutions that enable performance improvements, power efficiency, form-factor reductions and assembly excellence of current and next-generation semiconductor devices. Leveraging decades of development proficiency and extensive process technology expertise, Kulicke & Soffa's expanding portfolio provides equipment solutions, aftermarket products and services supporting a comprehensive set of interconnect technologies including wire bonding, advanced packaging, lithography, and electronics assembly. Dedicated to empowering technological discovery, always, K&S collaborates with customers and technology partners to push the boundaries of possibility, enabling a smarter future.

Booth: 36
LINTEC OF AMERICA, INC.
Phoenix, AZ
www.lintec-usa.com
LINTEC of AMERICA INC. Advanced Technologies Division 15930 S. 48th Street Suite 110 Phoenix, AZ 85048 Phone: 480-966-0784 Website: www.lintec-usa.com LINTEC is a worldwide leader in adhesive technologies. For 30+ years, LINTEC has created equipment and materials to solve difficult semiconductor process issues. With a catalog of hundreds of tapes and equipment, and decades of application experience, LINTEC is positioned to help. Whether you are looking for tape, need equipment to mount, peel or UV cure - our staff stands ready to assist you to provide the Adwill Advantage.

Booth: 31-32
MacDermid Alpha Electronics Solutions
Waterbury, CT
www.macdermidalpha.com
MacDermid Alpha supplies leading-edge technologies that enable the highest-end device designers and manufacturers to meet the evolving and demanding needs of the semiconductor industry.

Booth: 13
Metalor Technologies USA
North Attleboro, MA
www.metalor.com
Metalor Technology USA, a part of Tanaka Precious Metals family is uniquely positioned as the only global source of precious metal commodities and plating solutions with manufacturing sites and refineries throughout US, Asia, and Europe. Our comprehensive plating process range includes precious metal solutions and ancillary products. Metalor offers gold, silver, platinum, palladium, rhodium, ruthenium materials designed for use in semiconductor, electronic, and decorative applications. We offer a complete service; the supply of precious metal replenishment salts and anodes, process chemistry, as well as refining services can be your one-stop provider for precious metal needs. Our Technical Service Team, located facilities worldwide, is on call and equipped to provide rapid response to specific customer queries as well as on-site installation support.

Booth: 24
Micross Components
Apopka, FL
www.micross.com
Micross is a leading global provider of mission-critical microelectronic components and services for high-reliability markets. Micross provides a wide range of product and service solutions to customers, including Die & Wafer services, Advanced Interconnect Technology, Custom Packaging & Assembly, Component Modification Services, Electrical & Environmental Testing and other high-reliability products and services. In business for more than 40 years, Micross' extensive high-reliability capabilities serve the Aerospace & Defense, Space, Medical and Industrial markets, among others. Micross possesses the sourcing, packaging, assembly, engineering, test and logistics expertise needed to support applications throughout their entire program life cycles.

2023 Exhibitor Directory

Booth: 58
Mitsui Chemicals America
San Jose
https://us.mitsuichemicals.com/service/product/icros_tape.htm

"ICROS™ Tape" is a brand of tape designed for the semiconductor and electronic components manufacturing process flow, such as backgrinding (BG), compression molding, debonding, dicing/sawing, reflow, metal lift-off, protection for etching, CMOS image sensor handling, protection for back-metalizing, and etc. ICROS™ Tape has been the world's top protective tape used in semiconductor wafer BG for decades. Today, we offer tapes used for many other processes in the semiconductor and electronic components manufacturing flow. ICROS™ Tape is continuously evolving to keep up with the latest and future technologies in the semiconductor packaging process, such as temporary bonding/debonding for Fan-Out WLP/PLP, TSV wafer BG and dicing, Hybrid-bonding, Plasma dicing, and many other processes. We optimize the entire production process of our protective tapes from concept to raw material design to final inspection to meet the strict requirements of the semiconductor market. Everything takes place within a state-of-the-art clean room production facility with strict quality controls in place every step of the way. The result is ICROS™ Tape, for many applications, ultraclean tape with superior TTV (total thickness variation).

Booth: 14
MRSI Systems, Mycronic Group
Tewksbury, MA
https://mrsisystems.com/eng/

MRSI Systems (Mycronic Group) is the leading manufacturer of fully automated, high-speed, high-precision and flexible eutectic and epoxy die bonding systems. We offer solutions for research and development, low-to-medium volume production, and high-volume manufacturing of photonic devices such as lasers, detectors, modulators, AOCs, WDM/EML TO-Cans, Optical transceivers, LiDAR, VR/AR, sensors, silicon photonics, co-packaging optics, 3-D hybrid packaging, and optical imaging products. With 35+ years of industry experience and our worldwide local technical support team, we provide the most effective systems and assembly solutions for all packaging levels including chip-on-wafer (CoW), chip-on-carrier (CoC), PCB, and gold-box packaging.
For more information visit www.mrsisystems.com

About Mycronic

Mycronic is a Swedish high-tech company engaged in the development, manufacture and marketing of production equipment with high precision and flexibility requirements for the electronics industry. Mycronic's headquarters are located in Täby, north of Stockholm and the Group has subsidiaries in China, France, Germany, Japan, the Netherlands, Singapore, South Korea, United Kingdom, the United States and Vietnam. Mycronic is listed on Nasdaq Stockholm. www.mycronic.com

Booth: 41
NAMICS Technologies, Inc.
San Jose, CA
www.namics-usa.com

NAMICS is a global technology leader of advanced materials for semiconductor devices and packages, passive components and solar cells with over 75 years of experience and expertise. Headquartered in Niigata, Japan, NAMICS serves its worldwide customers with subsidiaries in the USA, Europe, Taiwan, Singapore, Korea, Hong Kong, and China providing unmatched worldwide support. Stop by booth # 41 to learn about NAMICS diverse product line of materials such as our packaging and board level underfills, low pressure liquid molding MUF for wafer level packaging, sintering technology for die attach and power devices, adhesives for sensor and camera modules and latest generation of functional materials for interconnects, heating, and bonding on flexible substrates. We build more than products; we build relationships, and NAMICS sets the gold standard for customer service by offering customizing products, world class customer support to provide a solution for your personal application.

Booth: 34
Noble Metal Services
Cranston, RI
www.NobleMetalServices.com

Reclaim of precious metals from your production materials. Supplier of gold, silver, and platinum. ITAR registered and fully EPA complaint. 100% destruction of your IP components.

2023 Exhibitor Directory

Booth: 53
NTK Technologies
Phoenix, AZ
www.ntktech.com

At NTK Technologies, we build robust packages for complex applications. However, our innovation helps to advance many of the technologies and products that improve people's lives. Computers, optical communication, wireless networks, medical devices, automotive, space and aeronautics -- many of the applications in these markets would not be possible without the technology that NTK provides. Whether it's IC packaging, peizoelectronics, ceramic filters, fine ceramics, or ceramic cutting tools, NTK is there providing these vital components that make it possible for the technologies that we use everyday to exist. NTK began with a superior expertise in ceramics. We are a part of NGK Spark Plugs, Co. LTD. (http://www.ngksparkplugs.com) which was founded in 1936. NGK Spark Plugs is a leader in the automotive industry with its advanced knowledge of technical ceramics. Through the years, our commitment to excellence evolved into an ambitious research and development program. NGK Spark Plugs' growing expertise in ceramic technology spawned the creation of NTK Technical Ceramics. In 1967, NTK Technical Ceramics embarked on the manufacturing of ceramic IC packages. From this endeavor, we have applied our technical expertise to expand into numerous industries including computers, communication, medical, avionics, and military applications. As a result we now specialize in more than just ceramics and have added various materials to our product offering, including organic substrates. Now known as NTK Technologies, we continue to add value to the market by developing industry-leading components for an endless amount of high-tech applications. Along with NGK Spark Plugs, Co. LTD, NTK is recognized all over the world as a premium brand. Our world headquarters is found near Nagoya, Japan (http://www.ngkntk.co.jp). We have sales offices and production facilities in six continents around the world. In the United States, we have seven sales offices with our head office and design center located in the Silicon Valley. NTK is an ISO9002/14001 (link to copy of the certificates) certified company. We are committed to providing our customers with the finest products and service possible. As the technologies in our lives continue to advance, NTK will be there providing the support necessary to achieve the visions of tomorrow.

Booth: 9
Okamoto Corporation
Santa Fe Springs, CA
www.okamoto-sed.com

Okamoto is a leading manufacturer of precision grinding and polishing tools. Okamoto builds some of the most precision tools in the world with thousands of world-wide installations. Machines built to customer specs for custom projects. Rigid design grinding tools built for wafer manufacturing of FOWLP, PLP, Strip, Cu, Resin, hard materials, SiC, sapphire, AlTiC, SOI, MEMS, Si, GaN, InP, Ge, GaAs, LT/LN, thin wafers to 50 microns or less, bumped wafers, and more. Patented (HPD) High Pressure Dressing technology make it possible to grind soft or hard materials with a high-mesh grinding wheel. NCG (Non-Contact Gauge) is also available. Polishing tools used with CMP technology, developed for high-throughput and high-accuracy. Fully-auto tools available up to 300mm. Also, a manufacturer for pitch polishers, slicers, and lapping machines.

Booth: 33
PacTech USA, Inc.
Santa Clara, CA
www.pactech.com

PacTech - Packaging Technologies GmbH (group member of NAGASE & CO. Ltd.) is headquartered in Germany with wholly owned subsidiaries: PacTech USA Inc. in Silicon Valley, USA, and PacTech ASIA Sdn. Bhd. in Penang, Malaysia. PacTech is comprised of three business units: EQUIPMENT MANUFACTURING: Manual & Automatic ENIG & ENEPIG plating tools, Laser soldeing equipment for balling and re-balling, Wafer-level solder ball transfer systems, Laser assisted flip-chip bonders. SUBCONTRACT SERVICES: Flip Chip and Wafer Level Package Bumping Services including ENIG or ENEPIG for UBM (solder bumping) or OPM (wirebond). Other services include Electroplating, Laser Solder Jetting, Solder Rework & Solder Reballing, Wafer Level Solder Balling, Re-passivation, RDL, Backmetal, Wafer Thinning, Wafer Dicing, Tape & Reel, AOI, X-Ray, SEM, FIB. CHEMISTRY: Pre-Treatment and process chemistry for electroless plating.

Booth: 55
Palomar Technologies
Carlsbad, CA
www.palomartechnologies.com

About Palomar Technologies Palomar Technologies makes the connected world possible by delivering a Total Process Solution™ for advanced photonic and microelectronic device assembly processes utilized in today's smart, connected devices. With a focus on flexibility, speed, and accuracy, Palomar's Total Process Solution includes Palomar die bonders, Palomar wire, and wedge bonders, SST vacuum reflow systems, along with Innovation Centers for outsourced manufacturing and assembly, and Customer Support services, that together deliver improved production quality and yield, reduced assembly times, and rapid ROI. With its deep industry expertise, Palomar equips customers to become leaders in the development of complex, digital technologies that are the foundation of the connected world and the transmission of data generated by billions of connected devices. Palomar solutions are utilized by the world's leading companies providing solutions for datacom, 5G, electric vehicle power modules, autonomous vehicles/LiDAR, enhanced mobile broadband, Internet of Things, SMART technology, and mission-critical services. Headquartered in Carlsbad, California, Palomar offers global sales, service and application support from its offices in the USA, Germany, Singapore, and China. For more information, visit: http://www.palomartechnologies.com

2023 Exhibitor Directory

Booth: 23
Practical Components
Los Alamitos, CA
www.practicalcomponents.com
Practical Components is an international supplier of Dummy Components, a large selection of advanced daisy-chain test die and wafers 40um to 200um pitch. Practical also supplies dummy SMT and Through-Hole components, qualification test PCBs, and solder training kits. Practical Components attempts to help solve the biggest problems in electronics: How to improve assembly quality, lower costs, and transition to new technology. Practical is an international supplier of products for many aspects of the electronics production chain, used everywhere from research to the production floor. Our customer base includes most major OEM, EMS, aerospace, automotive, government, medical, universities, and research sectors. Our unique products and services have built Practical Components' reputation globally since 1996. We utilize quality management standards to increase both business efficiency and customer satisfaction. Practical Components products solve problems, certify processes, introduce new concepts and help identify opportunities for product improvement.

Booth: 46
Promerus
Akron, OH
www.promerus.com
PROMERUS is a global leader in Cyclic Olefin Polymers (COP) and can provide advanced material solutions for your challenges in semiconductor, optoelectronics, electronic packaging, and emerging applications. As a subsidiary of Sumitomo Bakelite Co., Ltd., Promerus is well positioned to deliver our unique material sets to the market. At Device Packaging 2023, we are highlighting our low loss (Df <0.001 at 50 GHz), low dielectric constant (Dk <2.5) materials. We have versions that can be ink-jetted and others that can be applied via slot-die or spin coating. Visit us at Booth 46 to discuss your application requirements. We are here to develop materials tailored to your needs!

Booth: 43
QP Technologies
Escondido, CA
www.qptechnologies.com
At QP Technologies (formerly Quik-Pak), we offer a range of services to meet your packaging and assembly requirements. These include wafer preparation (backgrinding, dicing, die sort and inspection); IC assembly for a variety of package types and materials, as well as die attach, wire bonding, flip chip, encapsulation and marking; advanced assembly for new and complex packaging structures; laser micromachining; and design and engineering. In addition, we support design, fabrication, and assembly of PCB's for MCM and SiP applications. Our PCB supply chain is solid and supports FR-4 to ABF, fine line/spacing. We have added wire bond equipment to support heavy Al wire and challenging RF requirements. Please visit us at Booth #43 to discuss your needs and how we can apply our expertise and resources to support your project.

Booth: 64
Sales & Service, Inc.
Anaheim, CA 92807
www.salesandserviceinc.com
For over 30 years, Sales & Service, Inc. (SSI) has proudly provided Technical Solutions for Backend Assembly/Packaging & Test/ Inspection equipment, consumables, and services. SSI's Industry Leading line of suppliers include Solvay, Disco Hi-Tec America, Royce Instruments, Nordson, MicroPoint Pro, Boschman, Suron, and many more. Please visit SSI's Line Card for more information (https://salesandserviceinc.com).

Booth: 6
SETNA
Chester, NH
www.set-na.com
SETNA is the exclusive North American distributor of SET device bonding equipment. SET is globally renowned for the unsurpassed accuracy and the flexibility of its flip-chip bonders. Ranging from manual loading to fully automated version, the SET bonders adapt to all main bonding techniques: fluxless reflow, thermo-compression, adhesive joining compression, thermosonic... SET offers a comprehensive product portfolio of flip-chip bonders for fast growing markets and serving clients through a global network of representatives and in-depth customer trainings. Additionally, SETNA is also the North American distributor for Ontos Equipment Systems (OES) Atmospheric Plasma equipment. OES' Atmospheric Plasma Systems are used for surface preparation. It provides a simple, effective, clean surface modification method which does not require the throughput- robbing vacuum chamber associated with traditional plasma systems.

Booth: 49
Siemens
Wilsonville, OR
https://eda.sw.siemens.com/en-US/ic-packaging/
The pace of innovation in electronics is constantly accelerating. To enable customers to deliver life-changing innovations faster and become market leaders, Siemens is committed to delivering the world's most comprehensive portfolio of electronic design automation (EDA) software, hardware, and services

2023 Exhibitor Directory

Booth: 65
Silitronics
Santa Clara, CA
www.silitronics.com

Silitronics provides industry leading semiconductor IC package design and assembly services guided by "First Time Right" philosophy. Silitronics team has 100+ years of collective experience and expertise to propose, develop and implement cost effective design, layout, SI/PI, substrate fabrication and assembly solutions from concepts to finished products while exceeding specifications. Silitronics is centrally located in San Jose, the heart of Silicon Valley, and boasts a 10,000+ sq.ft. state of art automated facility with 10K and 1K clean rooms.

Silitronics' has fully automated equipment: Flip Chip with +/- 0.5um, Auto Dispensing and Pick/Place within +/- 3um, Automatic Wire Bonders to control 200um wire length and 50um loop height, Eutectic Attachment of Lasers and PCBA. Also, Silitronics capabilities includes Active Alignment for 8Chs, 19,000 Gold Stud Bump per die for Quantum Computing, 26,000 wires per SiP Modules, 8 ICs + 1 Interposer on a 15x15 package for Chiplets Integration. Many of the NPI package assemblies are so advanced that there is no precedence and does not fit in a standard assembly template. Often the design rules have to be pushed beyond their limits. This requires development of test vehicles, identification of right material sets, careful process control, monitoring of assembly parameters through well crafted DOEs and even investments in new equipment.

For Quality Control, 3-D Laser Microscope, Die Shear, X-ray, X-section and Wire Pull Tester in house. In house Machine Shop for fast cycle time. Silitronics also have ISO9001, ISO13485, ITAR, Mil Std 883 and Mil Std 38534.

Booth: 51
StratEdge Corporation
Santee, CA
www.stratedge.com

StratEdge Corporation, founded in 1992, designs, manufactures, and provides assembly services for a complete line of high-frequency and high-power semiconductor packages operating from DC to 63+ GHz. StratEdge offers post-fired ceramic, low-cost molded ceramic, and ceramic QFN packages, and specializes in packages for extremely demanding gallium arsenide (GaAs) and gallium nitride (GaN) devices. Markets served include telecom, VSAT, broadband wireless, satellite, military, test and measurement, automotive, clean energy, and down-hole. All packages are lead-free and most meet RoHS and WEEE standards. StratEdge assembly services have a Class 1000 cleanroom with Class 100 work areas for performing sensitive operations. It is fully equipped with the most modern assembly equipment, enabling high-speed, deep access, fine wire wedge and ribbon bonding. The component placement die attach system is the fastest and most reliable multiple die-type bonder on the market. It enables StratEdge to offer highly accurate, repeatable placement and includes a station for automated eutectic die attach utilizing proprietary processes that yield ultra-thin, low void solder joints. StratEdge has a variety of lids and options for their attachment and offers post assembly services. StratEdge is an ISO 9001:2015 certified and ITAR registered facility located in Santee, California, near San Diego.

Booth: 42
SUSS MicroTec Inc.
Corona, CA
www.suss.com

SUSS MicroTec is a leading supplier of equipment and process solutions for microstructuring in the semiconductor industry and related markets. Our portfolio covers a comprehensive range of products and solutions for backend lithography, wafer bonding and photomask processing, complemented by micro-optical components. In close cooperation with research institutes and industry partners SUSS MicroTec contributes to the advancement of next-generation technologies such as 3D Integration and Imprint Lithography as well as key processes for Wafer-Level Packaging, MEMS and LED manufacturing. With its global infrastructure for applications and service, SUSS MicroTec supports more than 8,000 installed systems worldwide.

Booth: 18
Technic
Cranston, RI
www.technic.com

Advanced Solutions for Semiconductor Manufacturing Technic supplies some of the most advanced solutions for semiconductor fabrication and packaging in the industry including electroplating chemistry, photoresist strippers, cleaners (post etch residue removers), metal etchants, and high purity wet chemistry, as well as semiconductor manufacturing equipment. High-performance product development, with application specific characteristics and unparalleled analytical expertise, provides customers with the essential tools to meet the challenges of today's semiconductor manufacturing.

Booth: 22
TechSearch International, Inc.
Austin, TX
www.techsearchinc.com

TechSearch International, Inc., founded in 1987, is a market research leader specializing in technology trends in microelectronics packaging and assembly. Multi- and single-client services encompass technology licensing, strategic planning, and market and technology analysis. Focus areas include flip chip, WLP, heterogeneous integration, chiplets, and substrates. TechSearch International professionals have an extensive network of more than 22,000 contacts in North America, Asia, and Europe. For more information, contact TechSearch at tel: 512-372-8887

2023 Exhibitor Directory

Booth: 7
Teikoku Taping System Inc.
Phoenix, AZ
www.teikoku-taping.com/en
Established in 1995, TTS is a leading manufacturer of Tape Lamination, Tape Removal, Wafer Mounting, and UV Irradiation equipment. In addition to wafer prep applications, TTS offers advanced, patented lamination of both Permanent and Temporary Dry Film Resist for cavities, microfluidic, and metallization applications. Additionally, we have implemented both patternable, Permanent as well as Temporary Wafer Bonding Tape, ABF, DAF, and Sheet Molding. TTS offers superior field support, as well as demo capabilities out of our US and Japan locations. Come by and see us, so we can discuss your advanced packaging needs.

Booth: 30
TOWA USA Corporation
San Jose, CA
https://www.towajapan.co.jp/en/
TOWA is a leading company in the semiconductor molding equipment market. We offer equipment using our high quality / flow free compression molding method and our proven transfer molding method. We also manufacture ultra-precision molds that have been highly acclaimed by customers. Together with our molding equipment, our singulation system was developed from both aspects of the dicer and product handler to provide the optimal method of singulation for each product type. The result is high quality cutting whilst improving customers' productivity with high throughput.

Booth: 2
Universal Instruments
Conklin, NY
www.uic.com
Universal Instruments offers contemporary, versatile, specialized solutions for next-generation assembly. Everything from - 2D, 2.5D, and 3D semiconductor applications requiring high accuracy and efficient die handling - to direct die and flip chip to multi-die heterogeneous integration. Our world-renowned Advanced Process Lab (APL) offers solutions for all aspects of a product lifecycle- from prototyping, process development, and analytical services to advanced technology assembly. Visit us, and let's discuss your advanced packaging challenges.

Booth: 61
XYZTEC, Inc.
Portsmouth, NH
www.xyztec.com
XYZTEC, Inc manufactures bond testers to the highest standard. We revolutionized test changeover with our Rotating Measurement Unit; eliminating cartridge exchanges. Our research and development efforts in recent years have been heavily focused on automation capability. The ROI is very quick when an operator does not have to be at the system 100% of their time. XYZTEC serves many markets including; microelectronics, automotive, battery, military, medical, solar and several non-traditional markets.

Booth: 59
Zuken, Inc.
San Jose, CA
https://www.zuken.com/us/
Zuken is a global provider of leading-edge software and consulting services for system-level electrical and electronic design and manufacturing. Founded in 1976, Zuken has the longest track record of technological innovation and financial stability in the electronic design automation (EDA) software industry for advanced packaging, printed circuit board design, and multi-domain co-design. The company's extensive experience, technological expertise and agility, combine to create world-class software solutions. Zuken's transparent working practices and integrity in all aspects of business produce long-lasting and successful customer partnerships that make Zuken a reliable long-term business partner. Zuken is focused on being a long-term innovation and growth partner. The security of choosing Zuken is further reinforced by the company's people— the foundation of Zuken's success. Coming from a wide range of industry sectors, specializing in many different disciplines and advanced technologies, Zuken's people relate to and understand each company's unique requirements.

Booth: 4
Zymet, Inc.
East Hanover, NJ
www.zymet.com
Zymet manufactures Adhesives & Encapsulants and has been serving the electronics industry for over 30 years. Products include reworkable underfills and edgebond adhesives for high reliability and harsh environment applications. Other products include ultra-low stress adhesives, electrically conductive adhesives, thermally conductive adhesives, and non-conductive pastes.

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Upcoming Events

Conference on Advanced Packaging for Power Electronics
Conference on High Temperature Electronics Conference
and
IMAPS/ACerS 18th International Conference and Exhibition on
Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT 2023)
April 18-20, 2023
Three Co-located Conferences: One location | One registration |
Three times the content, networking, and learning!

Conference and Exhibtion on Chiplet & Heterogeneous Integration Packaging Conference (CHIP)
(formerly our Advanced SiP)
July 24-27, 2023

Workshop on On-shoring Advanced Packaging and Assembly
July 10-12, 2023

EMPC 2023
September 11-14, 2023

IMAPS 2023 Symposium – San Diego
October 2-5, 2023

IMAPS 2024 Symposium – Boston
September 30-October 3, 2024

For more information, visit www.imaps.org or send your questions to info@imaps.org.

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Watch for dates to attend the 2024

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back in Arizona to celebrate the event's 20th Year!