iMAPS 2013

# 46th International Symposium on Microelectronics

## September 30-October 3, 2013

### Rosen Centre Hotel • Orlando, Florida, USA

**IMAPS2013.org**

Photo courtesy of Rosen Centre Hotel

**Final Program!**

## Highlights

**The most 2.5D & 3D Content Under One Roof:**
Featuring 3D Keynotes from Micron, CNSE, and TEL NEXX, and Panel Dicussion on *"What is Preventing 3D IC Integrations from High Volume Manufacturing?"*

6 "Best of Track" Outstanding Paper Awards & 1 "Best of Symposium"

Tuesday Keynote from Fraunhofer IZM and Wednesday Keynote from GLOBALFOUNDRIES

Monday & Thursday: 17 Professional Development Courses

30 sessions featuring more than 180 papers

Expanded Exhibits Tuesday-Wed. ONLY (Thursday tear-down)

NEW "Research Lab Corridor" on Exhibit Floor

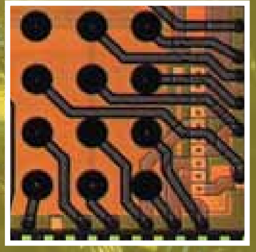
University Poster Session

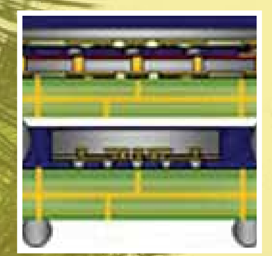
NEW GBC Market Forum Luncheon featuring keynote & market analysts

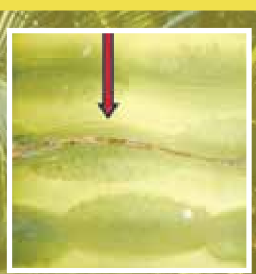
Dessert "Happy Hour" in the exhibit hall on Tuesday afternoon

Exhibitor Slideshows & Advertisements outside the session rooms

Exhibit Hall Reception Wednesday evening





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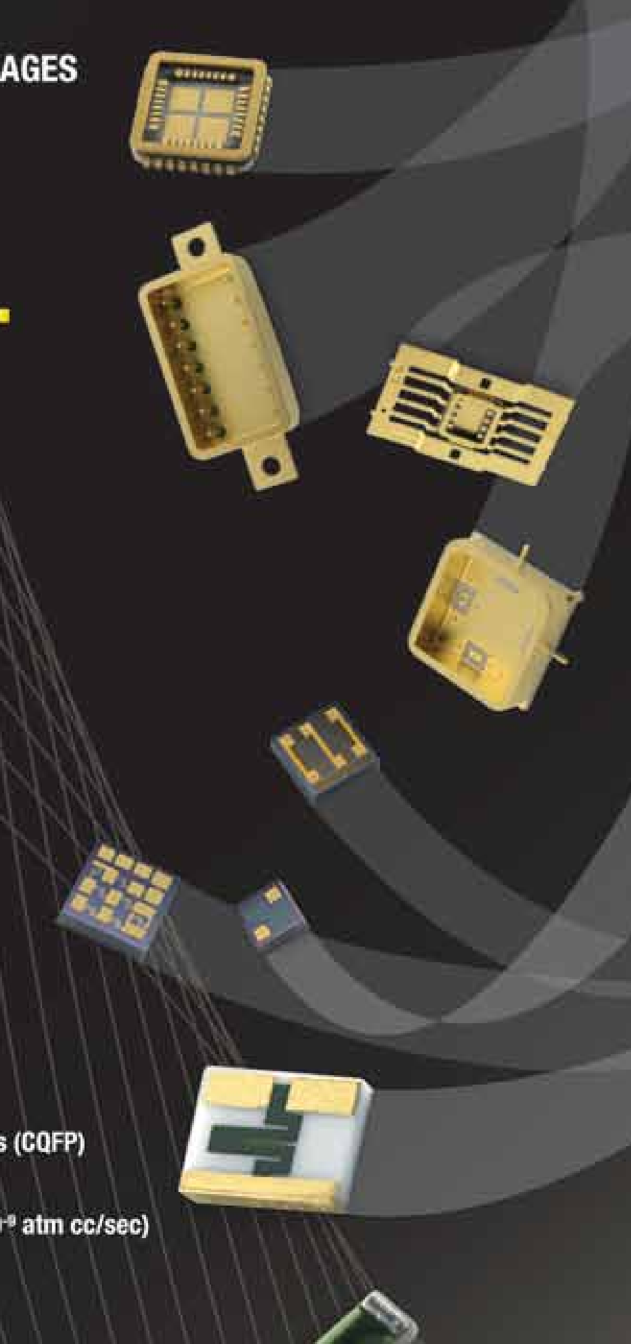

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### Professional Development Courses (PDCs):

***Monday, September 30: full-day courses, running 9:00 am - 5:00 pm;***
***Two half-day courses (8:00am - 12:00pm & 1:00 pm - 5:00 pm)***
***Thursday, October 1:all half-day courses, running 8:00 am - 12:00 pm***

### Registration:

Grand Ballroom Foyer

Monday, September 30 -- 7:00 AM - 5:00 PM
Tuesday, October 1 -- 7:00 AM - 6:00 PM
Wednesday, October 2 -- 7:00 AM - 6:00 PM
Thursday, October 3 -- 7:00 AM - 3:30 PM

### Technical Sessions:

Tuesday, October 1 -- 8:00 AM - 6:35 PM
Wednesday, October 2 -- 8:00 AM - 6:05 PM
Thursday, October 3 -- 8:00 AM - 4:10 PM

### Exhibition:

Grand Ballroom

Monday, September 30 -- SET-UP ONLY: 9:00 AM-6:00 PM
Tuesday, October 1 -- 11:00 AM - 5:00 PM
Wednesday, October 2 -- 9:00 AM - 7:30 PM
Thursday, October 3 -- MOVE-OUT ONLY: 8:00 AM - 2:00 PM

#### Photo Release

Photographs will be taken at the IMAPS 2013 Symposium. By registering for this meeting, you agree to allow IMAPS to use your photo in any IMAPS-related publications or website.

#### Loss Due to Theft

Symposium management is not responsible for loss or theft of personal belongings. Security for personal belongings is the responsibility of the individual.


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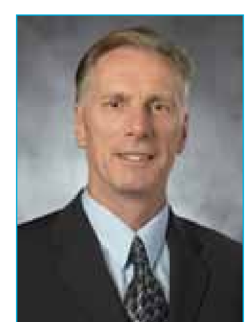
# Welcome from the General Chair



It's my honor to be this year's General Chair for the IMAPS 46th Annual International Symposium on Microelectronics. Thank you for joining us September 30th to October 3rd at the Rosen Centre Hotel in Orlando, Florida. IMAPS 2013 promises to be a special event with a strong technical program, and a large array of technology and manufacturing vendors at the exhibition hall.

The IMAPS committees and many dedicated volunteers have enhanced the 2013 program with exciting new features that provide added international flavor, and more learning and growth opportunities for you and your business. New on the 2013 program are a Research Center corridor in the Exhibit show floor, a full 3-day track on 2.5D/3D packaging, and expanded opportunities for students. We will also have an outstanding lineup of Professional Development Courses and an expanded roster of market presentations at the Global Business Council Forum.

This year's Technical Chairman, Ivan Ndip, has organized a team of co-chairs and session chairs for IMAPS 2013 and generated a strong program that will feature more than 180 technical papers on the latest research, development, and product advances. The technical program is organized into 6 parallel tracks and 30 sessions covering Advanced Packaging & Assembly, International Packaging and System Integration, 2.5D/3D Packaging, Modeling/ Design/Test/ Reliability, New Materials & Processing, and Emerging Technologies. Keynote speakers will be highlighted on each day of the symposium, and three keynotes and a panel on 2.5D/3D packaging technology will provide expert insights on the latest advances in this emerging field.

Be sure to visit the more than 125 exhibitors who will showcase a vast array of new products serving all segments of the microelectronics industry, including Military, Aerospace, Consumer, Mobile, Biomedical, Computing, Automotive/ Industrial, and Alternate Energy to find out the latest and greatest solutions to your needs in the supply chain.

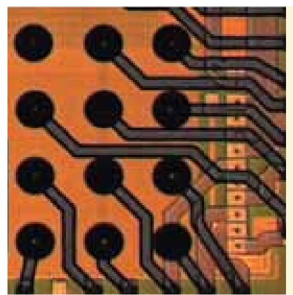
University students will have an opportunity to showcase their research and win prize money in a Student interactive poster session. And the IMAPS outreach program will facilitate a program with local high school students, giving students a chance to see what the microelectronics industry is all about.

To round out the activities, a fun golf tournament at Shingle Creek Golf Course will be held to help us on the "all work and no play" front.

It's been my pleasure to work with a diligent and steadfast organizing committee and IMAPS staff and a robust team of volunteers and co-chairs. They have assembled a superb program that truly brings the entire electronics supply chain together and I can't think of a better place to stay in tune than at IMAPS 2013 in Orlando. I encourage you take some time from your busy schedule to attend IMAPS 2013, to learn about a diverse scope of technology advancements, meet and collaborate with your peers, and create a network of new contacts from all over the world!

**Thank you for joining us this week!**

**Matt Nowak**
**Qualcomm Technologies, Inc**
**mnowak@qti.qualcomm.com**



# Welcome from Technical Chairs

Thank you for joining us in beautiful Orlando, Florida on September 30 – October 3, 2013 for the 46th International Symposium on Microelectronics (IMAPS). The annual IMAPS Symposium is well recognized as one of the premier international conferences for learning the latest advancements throughout the microelectronics packaging supply chain. This year, the Technical Program includes more than 30 technical sessions organized into 6 parallel tracks, plus keynote addresses, panels, and student activities. For the first time ever, the final manuscripts of the symposium will be peer-reviewed by the IMAPS Technical Committee. A Research Laboratory Corridor program is also introduced this year. This program provides an opportunity to promote cutting-edge research, fosters an expanded global network of collaboration between industry and R&D centers, and generates contacts for exploring technology transfer from the laboratories to the commercial, private and government sectors.

In addition to two days of Professional Development Courses, here is just a sample of the highlights for this year's symposium:

- top Keynote speakers from industry and academia
- full three-day track of special sessions presenting global perspectives of advanced packaging and system integration, including invited papers from Europe, Asia, and the USA
- full three-day track on interposers and 2.5D/3D packaging technology, including sessions on TSV materials and processes, glass interposers, technologies and methods for 2.5/3D packaging and integration. Advanced Platform Integration, and Packaging Transitions for 2.5D and 3D Interconnect.
- new sessions on Medical device packaging and on "Think Thin" packaging
- lively panel sessions with industry experts for hot topic discussions on 3D packaging
- engaging student posters session and numerous other student activities
- sessions to update us on the latest developments in package modeling, design, and reliability including design for reliability, testing techniques, reliability results, thermal management, signal integrity, and high performance interconnect
- full three-day track on advanced packaging materials including polymers, ceramics, encapsulants, and bonding materials
- the latest advances in Pb-free solder, flip chip, wafer bumping, copper pillars, wirebonding, and printed electronics
- practical insights on packaging applications including Microwave/RF, MEMS, optoelectronics, and LEDs
- research lab corridor on the exhibitor floor in which leading research institutions around the globe will be presenting their latest research results and future technology trends
- lots of awards including 6 "Best of Track" outstanding paper awards, 1 "Best of Symposium" award and student awards for best papers, booth and poster presentations

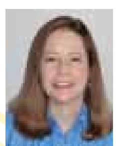
We gratefully acknowledge and extend sincere thanks to the IMAPS Technical Committee and IMAPS staff for their outstanding contribution to the 2013 program. We look forward to four days of creativity, innovation and networking.

**Ivan Ndip, Fraunhofer IZM**
**ivan.ndip@izm.fraunhofer.de**

*Technical Co-Chair - USA:*
**Mark Hoffmeyer**
**IBM Corporation**

*Technical Co-Chair - Europe:*
**Andre Rouzaud**
**CEA LETI**

*Technical Co-Chair - Asia:*
**Jin Yu**
**Korea Advanced Institute of Science and Technology (KAIST)**



*Assistant Technical Co-Chair - USA:*
**Erica Folk**
**Northrup Grumman**

*Assistant Technical Co-Chair - Europe:*
**Gilles Poupon**
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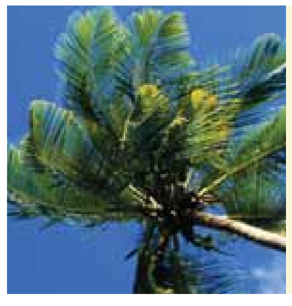

# Opening Ceremonies & Awards

## Opening Ceremonies

### Monday, September 30, 2013
### Welcome Reception

**5:00 PM - 7:30 PM • Jr. Ballroom F**
**Rosen Centre Hotel, Orlando, Florida**

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*Featuring Natel's First Annual Supplier of the Year Awards*

## Tuesday, October 1, 2013 | Opening Ceremonies:

**Rosen Centre Hotel • Jr. Ballroom F**

11:25 AM - 11:40 AM: Annual Business Meeting

11:40 AM - 12:00 PM: IMAPS Society Awards Ceremony

**Daniel C. Hughes, Jr. Award:** Sam Forman
**William D. Ashman Award:** John Lau
**John A. Wagnon, Jr., Technical Achievement Award:** Michael Osterman
**IMAPS Fellow of the Society:** Jin Yu; Matt Nowak; Adam Schubring; Shi-Wei "Ricky" Lee
**Outstanding Educator Award:** Douglas Hopkins
**Sidney J. Stein International Award:** Nihal Sinnadurai; Delip "Doug" Bokil
**Corporate Recognition Award:** Sikama International
**President's Awards:** Colin Johnston; Rajen Chanchani; Peter Elenius

### Best and Outstanding Papers - IMAPS 2012:

Zach Cole, Arkansas Power Electronics International
*Packaging of High Frequency, High Temperature Silicon Carbide (SiC) Multichip Power Module (MCPM) Bi-Directional Battery Chargers for Next Generation Hybrid Electric Vehicles*

Yiliang Wu, Xerox Research Centre of Canada
*Development of Silver Nanoparticle Ink for Printed Electronics*

### Best Paper - IMAPS 2012:

Thomas Brunschwiler, IBM Research
*Formulation of percolating thermal underfills by hierarchical self-assembly of micro- and nanoparticles by centrifugal forces and capillary-bridging*

Come say *Thank You* to those who contributed so much to IMAPS over many years.

**Keynote Presentation: 12:00 PM - 12:45 PM**

### Next Generation of Electronic Systems - Challenges and Solutions for System Integration Technologies

Prof. Dr. -Ing. Dr. sc. techn. **Klaus-Dieter Lang** - Klaus-Dieter Lang is a Professor with the School of Electrical Engineering and Computer Sciences at the Technical University Berlin, Germany, where he leads research activities in the area of Nano Interconnect Technologies. He is also the Director of the Fraunhofer Institute for Reliability and Microintegration, IZM, Berlin.

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# Micross Components: Plant Tour

Micross Components will provide a valuable industry tour that will highlight two of their facilities in Orlando. Micross Components is a leading global provider of distributed and specialty electronic components for military, space, medical, and demanding industrial applications. Operating as a single source for high reliability and state of the art electronics, Micross™ solutions range from bare die and wafer processing to advanced and custom packaging to component modifications and related interconnect offerings. With a 35+ year heritage, Micross possesses the design, manufacturing and logistics expertise needed to support an application from start to finish. **The plant tour is set for Wednesday, October 2: bus leaving Rosen Centre at 11:30am and returning by 2:00pm. Preregistration has closed. See Brian or Brianne at the registration desk for details about the tour and to meet the bus.**

***The Micross Tour is open to US Citizens ONLY. Students and industry professionals are welcome to participate. Micross will manage the approved attendee list and communicate with registrants as the tour approaches.***

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# Professional Development Courses (PDCs)

## NEW PDC FORMAT THIS YEAR - Monday & Thursday Courses

### Monday PDCs: full-day courses, running 9:00 am - 5:00 pm unless otherwise noted

### All Thursday PDCs are half-day, running 8:00 am - 12:00 pm

Do you want to broaden and strengthen your skills and knowledge, optimize your manufacturing processes, and integrate the latest advances in materials and technologies to maintain your strength in today's competitive global market? The Technical Committee of IMAPS is pleased to present a comprehensive offering of Professional Development Courses that provide detailed information on topics of immediate interest to the Microelectronics and Packaging community. So please be sure to choose from the 17 in-depth Professional Development Courses taught by recognized industry experts. You will discover the following key ways that will benefit you.

- **Better understand the skills and knowledge necessary in today's industry.**
- **Be exposed to the rapidly expanding developments in new materials and technologies.**
- **Consult with renowned authorities about your current R&D or manufacturing problems and challenges.**
- **Learn new ways to identify, think about, and address your problems and opportunities.**
- **Great opportunities to interact with industry experts and other course attendees.**
- **Courses now offered Monday and Thursday so you can attend a course without missing the conference or extending your travel plans!**

### Your PDC Registration Fee Includes:

- Lunch on the day of your course (Monday full-day PDCs only)
- Refreshment breaks
- Hard-copy workbook of course materials (no electronic copies provided)
- Attendee list following your course

#### PDC Cancellation policy:

*IMAPS reserves the right to cancel a course if the number of attendees is not sufficient.*
*You can transfer to a different course or we will refund you the corresponding amount.*

## Monday PDC Lunch sponsored by:

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# Monday, September 30, 2013

## Monday PDCs run 9:00 am - 5:00 pm unless otherwise noted

| | |
|---|---|
| **PDC Coffee Break in Salon Foyer:** | **10:00-10:15 am** |
| **PDC Lunch in Salon 11-12:** | **12:00-1:00 pm** |
| **PDC Afternoon Coffee Break in Salon Foyer:** | **3:00-3:15 pm** |

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### M1A: Plating Processes for High Rel Microelectronic Devices
### PDC Instructor: Fred Mueller, General Magnaplate Corp.

### 1/2 Day Course (4-hour): 8am-12pm — Salon 1

**Course Description:** Review the engineering differences and troubleshooting problems in the plating processes used in Plating for Electronics... - Comparison of Electroless Nickel / Immersion Gold (Ni/Au), Electroless Nickel / Immersion Silver (Ni/Ag) and Electroless Nickel / Electroless Palladium / Immersion Gold (Ni/Pd/Au) processes - Presents methods for controlling the properties of plating solutions to maximize the deposits properties, including Laboratory Controls / Equipment - Electroless Nickel/Immersion Gold, Solderability and Solder Joint Reliability as Functions of Process Control - What lack of ENIG process controls can result in black pad? - Flip Chips: review of electroplated solders and golds and newer technology - electroplated copper-bumped wafers.

### M1B: Fundamentals of Glass Technology and Applications for Advanced Semiconductor Packaging
### PDC Instructor: Dr. TJ Kiczenski, Corning Incorporated

### 1/2 Day Course (4-hour): 1pm-5pm — Salon 1

**Course Description:** The objective of this course is to build a foundation of understanding of engineered glass as a material that technologists can leverage in the development of advanced IC packaging applications. Starting from the fundamental principles of glass structure, composition and properties we will provide a broad overview of glass with a focus on unique attributes that make glass as an enabling material. Subjects to be covered will include strength and reliability, chemical durability, thermal behavior, associated thermal relaxation behavior, and electrical properties. Additionally we will review the platform alternatives as part of the "glass toolkit" available to semiconductor packaging development including various manufacturing (melt & form) approaches, the diversity of compositional options and a survey of glass processing options that can be adapted from adjacent glass technology space to advanced semiconductor packaging. Finally the course will illustrate with case studies how glass is contributing to emerging 3D-IC technologies and explore current and potential applications in advanced semiconductor packaging. We will focus on its role as a carrier for temporary bonding, integrated wafer for CMOS Image Sensor, and 2.5D and 3D glass interposers. Relative costs of glass will be discussed as an alternative to other materials for carriers and interposers.

### M2: Polymers in Electronic Packaging
### PDC Instructor: Dr. Jeffrey Gotro, InnoCentrix, LLC

### Salon 2

**Course Description:** The course will provide an overview of polymers and the important structure-property-process-performance relationships for electronic packaging. The main learning objectives will be 1) understand how polymers are used in electronic packaging, 2) learn why specific chemistries are used depending on the application 3) learn the fundamentals of polymer characterization related to electronic packaging 4) develop a foundation in rheology and rheology issues in electronic packaging.

Topics to be covered are thermosetting polymers, curing mechanisms (heat and light cured), network formation, and an overview of key chemistries used (epoxies, acrylates, polyimides, bismaleimides, curing agents, and catalysts). The course will provide a more in-depth discussion of the chemistries, material properties, and process considerations for adhesives (both paste and film), capillary underfills, packaging substrate materials, encapsulants (mold compounds), and coatings. Characterization using thermal analysis will be covered allowing understanding of structure-property relationships. The final portion of the PDC will provide an introduction to rheological characterization methods (various types of rheometers and viscometers) and the properties of adhesives (shear thinning, viscosity, time dependence, and rheology changes during curing), underfills, and mold compounds. Participants are invited to bring problems for discussion.

## Salon Rooms 1-10

## M3: Wire Bonding in Microelectronics: Materials, Processes, Reliability and Yield
## PDC Instructor: Lee Levine Process, Solutions Consulting, Inc.

### Salon 3

**Course Description:** Wire bonding is the dominant method for chip interconnection. This year the semiconductor industry will produce over 1312(13 trillion) wire bonds. As a result of the increase in the cost of gold a significant portion (approximately 15%) of the entire market has already converted to copper ball bonding. A comparison of the costs, reliability, and difficulty of copper ball bonding will be included. The objective of the short course will be an understanding of the process from the metallurgy to process optimization and capillary selection.

- The Ball Bond Process: Step by Step Wire Bonding
- Welding
- The effect of ultrasonics on weld formation and materials properties
- Metallurgy and Intermetallics
- A comparison of the welds associated with Au-Al and Al-Cu bonding
- Au-Al failure mechanisms in ultra-fine pitch bonding
- The effect of wire alloying on ultra-fine pitch reliability
- Wire properties, testing and chemistry
- Pull and shear testing wire bonds
- Long term accelerated testing of wire bonds
- Understanding wire stiffness and the effect on looping
- Wire bond loop shapes
- The second bond
- Diffusion
- The principal bonding variables
- Capillary design and selection for optimized processes
- Simple bond screening designed experiments
- How to optimize the bonding process

## M4: Technology of Screen Printing
## PDC Instructors: Art Dobie, Sefar Inc.; David Malanga, Heraeus, Inc., Thick Film Division

### Salon 4

**Course Description:** Screen printing continues to offer innovative and cost effective solutions to the increasing demands for higher circuit densities. This course is intended to increase the understanding of the screen printing process, thereby improving production yield and print quality.

Presented are some of the latest advancements in composition, screens, and printing technology that enable screen printing to meet future circuit density requirements as well as the definition required for microwave circuitry. The advantages of screen printing, an additive deposition process, are described and compared to alternative more costly and “less-green” subtractive deposition technologies. This course is applications-oriented in terms of how to optimize the screen printing process; how to use and specify screen correctly; rheology properties that affect print results; minimizing printing defects and trouble-shooting problems related to screens, inks and the printing process itself.

## M5: Recent Advances and New Trends in 3D IC Integration
## PDC Instructor: John H. Lau, ITRI

### Salon 5

**Course Description:** 3D integration consists of 3D IC packaging, 3D IC integration, and 3D Si integration, which will be discussed in this lecture. Emphases are placed on the key enabling technologies for 3D IC integrations, such as TSV (through-silicon via) forming and filling, front and back-side metallization, RDL (redistribution layer), temporary wafer bonding, wafer thinning and handling, wafer de-bonding, thin chip/wafer strength measurement and improving, lost-cost lead-free microbumping ($<=15\mu m$ pitch) and assembly, C2C, C2W, and W2W bonding, and thermal management. Useful characterization and reliability data for 3D IC integration will also be provided. The application of 3D IC integration such as MEMS, LED, logic + logic, memory + microprocessor, wide I/O DRAM, active and passive interposers will be presented. Furthermore, the critical issues of TSV and 3D IC integration will be given and some potential solutions or research topics will be recommended. Finally, the supply chains for high volume manufacturing of 3D IC integration will be discussed and several roadmaps of 3D IC integration will be provided. All the materials are based on the technical papers and books published within the past 3 years by the lecturer and others.

**Salon Rooms 1-10**

## M6: 2013 Packaging Advances, Updates and Trends
## PDC Instructor: Phillip G. Creter, Creter & Associates

### Salon 6

**Course Description:** This NEW overview course focuses on 2013 packaging topics, reviewing leading edge developments in microelectronics advances/updates/trends. Abstracts are expanded from 2013 papers to highlight technical innovations, adding selected tables, photos, figures, conclusions, recent news reports, and organized into the following technical groups:

- 2.5D-TSV Interposers (wafer-level encapsulation, underfill, through-glass-vias using electric discharging, ultra-thin die stacking, warpage control)
- 3D-TSV (through-silicon-stack for Wide I-O, heterogeneous CoWoS, self-assembly, low-cost chip-on-chip, low temperature Cu-Cu bonding, temporary wafer bonding)
- Chip-Package-Interactions (ultra-thin chip stacking/packaging, stress testing, warpage design/control, coreless substrates)
- Flip Chip (fine-pitch/micro-pitch copper pillars, predicting electromigration reliability, large die on coreless, non-conductive adhesive for micro-pitch, thermally-enhanced FC)
- LED (very high power density, high-brightness substrate-reflectivity study, nano-composites, quasi-conformal phosphor dispensing, ultra-thin wafer-level-packaging)
- MEMS (hermetic wafer-to-wafer bonding, carrier wafer with self-assembled monolayer, outgassing, low-cost sensor, high temperature SiC MEMS)
- Microbumps (minimizing electromigration, effect of plating on microbump reliability, design rules, key elements of sub-50 um microbumps, micro-solder bumps)
- New Adhesives (Ultra-Fine-Pitch adhesives, micro-pitch interconnects using ACF, NCF wafer lamination, high-thermal conductive ACF, isotropic conductive adhesive using micro-spheres)
- Embedded Chips (microprocessor/capacitors, WLCSP, wafer/panel mold embedding, reliability, capacitor-embedded interposers)

Technical innovations presented with input from leading industrial/academic institutions: Amkor, Asahi Glass, ASE, Cisco, Fairchild, Fraunhofer IZM, Georgia Institute of Technology, Huazhong University, Hynix, IBM , IMEC, Infineon, Intel, ITRI, Kaist, NAMICS, Qualcomm, Samsung, SEMATECH, SPIL, STMicroelectronics, Sumitomo, Suss MicroTec, Taiwan Semiconductor, Tohoku University, Xilinx, Yole, others.

## M7: Introduction to 3D Power Electronics & Post-Silicon Device Packaging
## PDC Instructor: Dr. Douglas C. Hopkins, North Carolina State University

### Salon 7

**Course Description:** Power densities and switching speeds in power electronics applications have increased well over ten fold in the last three years. With the advent of post-silicon power devices, i.e. SiC, GaN and GaAs, voltages and current densities are at unprecedented levels. The greatest change is in switching speeds that approach gigahertz. All this, and operating temperatures are pushing above 250C.

This course is an excerpt from a 45-hour university graduate course that introduces the evolving characteristics of the post-silicon devices; new "energy electronics" packaging materials; and new 3D printed power-packaging technologies. This daylong course presents a comprehensive approach from defining the new challenges facing power packaging to new packaging techniques for working at higher temperatures.

Half the course details more traditional power packaging techniques, such as directed-bonded-metal (Al - DBA and Cu - DBC) and limitations on their applicability to the new higher temperatures and speeds. The other half shows how microelectronics packaging technologies, such as 3D printing, and stack die and stacked boards, can be used in power applications for point of load converters, etc.

## M8: Hermeticity Testing of Microelectronics for Aerospace and Medical Applications
## PDC Instructor: Thomas J Green, TJ Green Associates LLC

CANCELLED

### M9: Reliability Data Analysis
### PDC Instructor: Jianbiao Pan, California Polytechnic State University

#### Salon 9

**Course Description:** The objective of this course is to introduce the fundamentals of reliability concepts and enable the student to analyze reliability data and interpret the results. A hands-on training using statistical software Minitab or JMP will be provided as well.

**Course outline:**

- Basic reliability concepts
  - The definition of reliability, MTBT, MTTF, failure rate, hazard rate, and bathtub-curve.
  - Different data types: right censored, interval censored, left censored, uncensored.
  - The most commonly used distributions in reliability engineering: exponential, lognormal, and Weibull.
- Reliability data analysis
  - Reliability distribution identification: probability plotting
  - Parameter estimation
- System reliability

At the end of this course, participants should be able to:

- Describe basic reliability concepts and bathtub-curve; distinguish reliability data characteristics; and estimate reliability terms using empirical reliability data.
- Fit statistical distributions using statistical software JMP or Minitab and interpret the failure mode based on estimated Weibull parameters.

Students are asked to bring along laptop computers with JMP or Minitab (free trial version available) to use during class.

### M10: MEMS Reliability and Packaging
### PDC Instructor: Slobodan Petrovic, Oregon Institute of Technology

#### Salon 10

**Course Description:** This course provides a comprehensive discussion of a broad array of MEMS packaging and reliability issues. An overview of the principles of operation, fabrication methods, and materials used in building MEMS structures will be presented as well. Because each MEMS device requires a distinctive packaging approach, practical examples and illustrations will be used to demonstrate uniqueness of solutions and interactions between micromachined structures and packaging.

A full range of MEMS devices will be discussed while a particular emphasis will be placed on sensors and actuators used in industrial, medical, and automotive applications. Extensive case studies that will be used to most effectively demonstrate diverse packaging principles for devices such as accelerometers, pressure sensors, and digital micromirror devices.

The course will be divided in 2 major sections: general MEMS competence; and packaging and reliability. The following major topics will be covered: fabrication technologies, materials, device physics, design considerations, main MEMS types, integration aspects, selected industrial application, types of packaging, quality control, reliability and failure analysis.

**NEW THIS YEAR!**

**THURSDAY PDCs. THERE IS STILL TIME TO REGISTER FOR THE FOLLOWING COURSES...**

# Thursday, October 3, 2013

## All Thursday PDCs are 1/2 Day Courses (4-hours): 8:00 am - 12:00 pm

**10:15 AM - 10:30 AM: Coffee Break In Ballroom Foyer**

*IMAPS Cafés sponsored by:*

### T1: Package on Package Technology - What It Is, What Works, What Doesn't Work
### PDC Instructor: Dr. Ning-Cheng Lee, Indium Corporation

**Salon 2**

**Course Description:** This course covers Package on Package (PoP) Technology, including trends, designs, material selection, processes, and reliability. The approaches of enhancing the reliability will be discussed in details, including effect of fluxes, solder alloy types, processes, profiles, via designs, and ball sizes. Being the solution with the highest potential, epoxy flux will be introduced and will be compared with other solutions. Finally, head in pillow control at reflow soldering, particularly at PoP will be instructed. The control includes considerations on materials, processes, and designs.

**Course Content:**

- Trends
- Designs
- Processes - General
- Processes - Rework of PoP
- Processes - Selection of Dip Transfer Fluxes and Solder Pastes for PoP Assembly
- Processes - Low Volume PoP Assembly Process Development
- Processes - Design for Efficient PoP Underfilling
- Processes - Comparison of Various Polymeric Reinforcement Approaches for PoP/CSP
- Reliability - One-Pass vs Two-Pass
- Reliability - Effect of SOP & Material on Yield & Drop Test Performance
- Reliability - Effect of Materials & Profiles
- Reliability - Materials Selection & Parameter Optimization
- Reliability - Mixed Alloy
- Reliability - Effect of Coplanarity and Design
- Reliability - Effect of Ball Size, Via Size, Alloy Type on Stack-up Height & Reliability
- Reliability - Opens/Head-in-Pillow - The Primary Failure Mode of PoP

**Who Should Attend?** Anyone who cares about successful implementation of package on package technology, and like to know how to achieve it should take this course.

**Ning-Cheng Lee** *is the Vice President of Technology of Indium Corporation of America. He has been with Indium since 1986. Prior to joining Indium, he was with Morton Chemical and SCM. He has more than 20 years of experience in the development of fluxes and solder pastes for SMT industries, plus experience in underfills and adhesives. He received his PhD in polymer science from University of Akron in 1981, and BS in chemistry from National Taiwan University in 1973. Ning-Cheng is the author of "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies", and co-author of "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials". He was honored as 2002 Member of Distinction from SMTA, 2003 Lead Free Co-Operation Award from Soldertec, 2006 Exceptional Technical Achievement Award from CPMT, 2007 Distinguished Lecturer from CPMT, 2009 Distinguished Author from SMTA, and 2010 Electronics Manufacturing Technology Award from CPMT.*

### T2: Flexible Optical Media for High Data Rate Interconnections
### PDC Instructor: Dr. How T. Lin, Endicott Interconnect Technologies, Inc

**CANCELLED**

### T3: Understanding the Common Failure Modes from a Physics of Failure Perspective
### PDC Instructor: Greg Caswell, DfR Solutions

### Salon 4

**Course Description:** There are numerous failure modes and mechanisms that can impact a product. Understanding how they occur and how to obviate them during the design stage can vastly improve a product's ability to withstand the rigors of its intended environment.

This course will address the common failure modes associated with printed circuit boards,passive components, Integrated Circuits, High Brightness LEDs, QFNs, CSPs, PoP, and MEMs along with the effects of long term storage of components.

Physics of Failure (PoF) is a proactive science based philosophy that addresses material science, physics and chemistry and provides the basis for the student to develop an up-front understanding of failure modes/mechanisms. Knowing how things fail is equally important to understanding how and why things work by enabling engineers and designers to be knowledgeable about root causes of failures so that they can be designed out in new products.

PoF provides a scientific basis for evaluating usage life and hazard risks for new materials, structures and technologies when exposed to their actual operating conditions.

Examples of each failure mode/mechanism will be illustrated along with insight into methods for obviating them.

**Who Should Attend?** Engineers or designers who are developing new products and want to understand how to enhance their designs by developing an in depth knowledge of the various issues that can impact a product design if the wrong materials, packaging technologies, stress loads, or manufacturing processes are implemented.

**Greg Caswell** *is widely recognized as a pioneer in surface mount technology (SMT) and has 40 years of experience in the electronics industry. Currently he is a Sr. Member of the Technical Staff for DfR Solutions. Previously he was the VP-Engineering for Reactive NanoTechnologies and VP Business Development for Newport Enterprises. His experience encompasses all aspects of SMT manufacturing, circuit board fabrication and materials, advanced packaging (BGA, uBGA, CSP, Flip Chip, QFN), IC fabrication processes and materials, solder reflow, RoHS, and bonding utilizing specialized nanotechnology. Greg, a Past President of IMAPS NA, was the National Chairman for the IMAPS Advanced Technology Workshop program from 1989-2000 and was the Editor in Chief for Advancing Microelectronics magazine from 2009-2012. He received his Bachelor of Science in Electrical Engineering from Rutgers University and also has a Bachelors in Management from St. Edwards University in Austin.*

**Salon Rooms 1-10**

## T4: Embedded Chip Packaging Technologies
## PDC Instructor: Ray Fillion, Fillion Consulting

### Salon 5

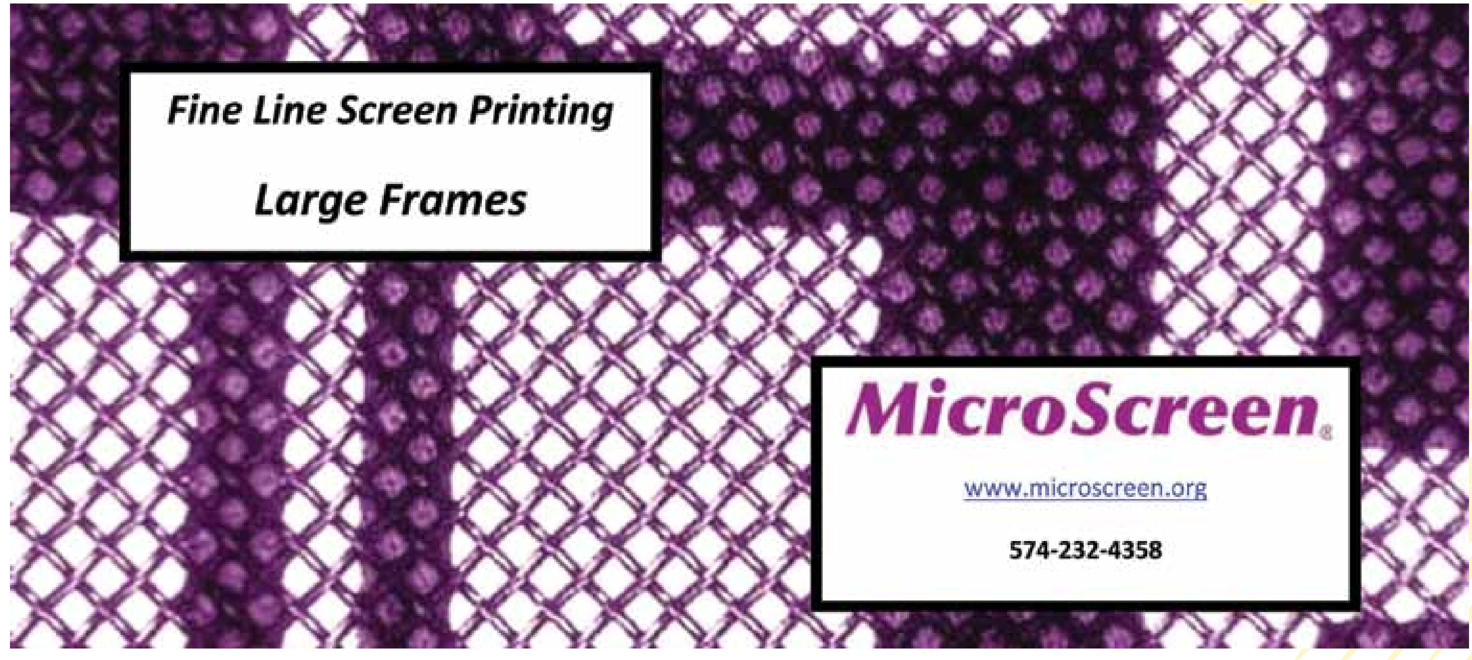
**Course Description:** Semiconductor process and device advances have provided ever more functionality in a smaller chip footprint and have driven both the high-end computing market and the portable electronics market. Advances in microelectronics packaging have become just as critical to these markets. These device advances come with an increase in device power requirement, cooling needs, I/O counts and voltage delivery sensitivity. Embedded chip approaches have been developed to address these devices advancements and packaging needs. This course will give an in depth look into embedded chip technologies.

It will start with a background overview of semiconductor advances for the past 40 years and they are effecting device power dissipation, supply current, I/O count and clock rate. It will look at the evolving packaging approaches that have occurred over the past 20 years. It will go into the various approaches used in SoP, SiP, MCP and MCM multichip technologies; 3-D technologies; wafer level package. This course will focus on single chip and multichip embedded chip technologies.

It will look at the basic features of embedded chip approaches, their construction and the processes used to fabricate and assemble them. It will look at the leading approaches to these technologies and their inherent advantages and disadvantages. This course will cover issues including yield losses, component handling and availability. The course will look at the leading companies implementing various versions of these technologies and cover the key differentiators between them.

**Who Should Attend?** This course covers basic and advanced topics for product and design engineers, manufacturing process and assembly/packaging engineers, engineering managers, senior design technicians, consultants and academic specialists as well as marketing and sales personnel requiring an understanding of the capabilities, implications and options of advanced packaging and assembly technologies.

*A BSEE graduate of University of Massachusetts,* **Ray Fillion** *focuses in the areas advanced packaging and interconnection for next generation microelectronics systems. Ray has more than 40 years experience at GE in Aerospace Electronics and Global Research in all aspects of microelectronics in technical, management, business development and IP licensing positions. Mr. Fillion also has served on Advisory Boards for a variety of technical societies, industry, academic institutions and governmental funded agencies. He has taught courses on advanced packaging for IMAPS, SMTA, GE and several universities. Ray is now heads a consulting firm, Fillion Consulting, specializing in technical assessment of microelectronic technologies and IP including multichip modules, chip scale, 2.5D/3D, embedded chip and power packaging. He was the lead inventor of the GE embedded chip technology with most of his 32 issued US patents in that area. He has been active in a number of technical societies including IMAPS: Executive Council Director, Technical Committee Member, Session Chair, Presenter; ECTC: Technical Committee Member, Session Chair, Presenter; and Symposium of Polymers in Microelectronics: Board Member, Session Chair, Presenter. He has authored more than 125 technical papers, journal papers, and technical articles with three Outstanding Paper awards from the IMAPS International* Conference.




Salon Rooms 1-10

### T5: Practical Aspects of MEMS and Microsystem Packaging
### PDC Instructor: Chip Spangler, Aspen Microsystems

#### Salon 6

**Course Description:** MEMS and Microsystem devices have seen remarkable growth in both high-volume commercial applications as well as lower-volume specialty applications. One of the key reasons for this growth is the advances made in package technologies and the related reductions in cost and improvements in device function that they enable. This class will provide practical guidance for those looking to leverage these advanced packaging technologies to help bring their products to market. The first portion of the class will set the context for microsystem packaging by exploring a diverse range of real-life applications and the packaging challenges they present. Case studies will be used for this exploration into inertial sensors, micro-displays, RF switches and components, print heads and fuel cells as well as medical packages for neural stimulation and DNA analysis. These case studies will focus not only on package design and system interfaces, but also the material and assembly process challenges they create. The second portion of the class will review the fundamentals of microelectronic package design and assembly process as adapted for MEMS and microsystem applications. Topics will include wafer dicing, die attach, wirebond and flip chip technologies as well as hermetic sealing and non-hermetic encapsulation methods.

**Who Should Attend?** This course is intended for designers, engineers and technical managers who would like to learn about practical aspects of packaging MEMS and microsystem devices. Through real-life case studies attendees will be given the tools needed to analyze the technical tradeoffs so that the products they are responsible for will meet functional, cost, reliability, size and quality requirements. This course will also be suitable for those who are looking for a broad introduction into the challenges of MEMS packaging. Practical information regarding materials, equipment and processes will provide a solid foundation for attendees to address the packaging challenges in their organization.

**Dr. Chip Spangler** *received his Ph.D. in electrical engineering from The University of Michigan in 1988. He is currently President of Advanced Microsystems providing engineering services for advanced microelectronic devices, with specialties in MEMS package and assembly technologies. Previously Chip was the President and CTO of Aspen Technologies, a microelectronic package and assembly service supplier. He was responsible for developing package solutions for high-pixel count displays, DNA analysis products and MEMS telecom switch arrays as well as a variety of other MEMS devices. Before this, Chip worked at Ford Microelectronics where he had responsibility for pressure sensors, and airbag and chassis accelerometers. His work lead directly to the production of the worldÃ¢â‚¬â„¢s first plastic surface mount airbag accelerometer. Dr. Spangler is the author of over 30 technical publications and has 9 patents. He is currently an editor for IEEE JMEMS and has helped organize a number of MEMS technical conferences.*

### T6: Signal/Power Integrity Design for Electronic Packaging and 3D System Integration
### PDC Instructors: Dr. Ivan Ndip, Fraunhofer IZM; Professor Ege Engin, San Diego State University; Dr. Antonio Ciccomancini Scogna, CST of America

#### Salon 7

**Course Description:** Efficient and low-cost design of electronic packages, PCBs and 3D integration technologies requires a good understanding of the root causes of signal integrity (SI), power integrity (PI) and electromagnetic interference (EMI) problems at GHz frequencies, as well as methods to analyze, prevent or solve them. The objective of this course is to illustrate a wide range of methods for electrical modeling, measurement and optimization of electronic packages, PCBs and 3D integration technologies, under consideration of SI, PI and EMI/EMC effects. Measurement techniques for extracting the relative dielectric constant and loss tangent of electronic packaging materials will also be discussed. Finally, design guidelines for system optimization will be provided.

**Course Outline:**

- Introduction
  - o Technologies for advanced packaging and 3D integration
  - o High-speed design challenges
- Signal Integrity Design and Optimization
  - o Lossy transmission lines considering surface roughness and glass weave effect
  - o Signal vias in organic and glass interposers
  - o Through silicon vias (TSVs) in active and passive silicon for 3D integration

- Efficient methods for performing signal integrity simulations, considering package/PCB co-simulation

- Power Integrity Design and Optimization
  - Power-ground plane pairs
  - Decoupling capacitors and simultaneous switching noise (SSN)
  - Electromagnetic band gap (EBG) structures and photonic crystal power/ground layers (PCPLs) for suppressing SSN coupling
  - Efficient methods for performing power integrity simulations
- Measurement and extraction of relative dielectric constant and loss tangent of packaging materials.

**Who Should Attend?** Engineers, scientists, researchers, designers, managers and technicians involved in the process of layouts, simulation, design, integration and optimization of electronic packages, PCBs and interconnections.

**Dr. Ivan Ndip** *obtained his M.Sc., and Ph.D. with the highest distinction (Summa Cum Laude) in electrical engineering from the Technical University Berlin, Germany. In 2002, he joined the Fraunhofer-Institute for Reliability and Microintegration (IZM) Berlin as a Research Engineer and worked on signal integrity modeling and design as well as on antenna integration. Since 2006, he has been a Senior Research Engineer and Group Manager of RF & High-Speed System Design, where he's responsible for leading a team of Research Engineers and Graduate Students as well as for developing and leading research projects that focus on electromagnetic modeling, design and optimization of RF/high-speed packages/boards/modules, integrated antennas and passive RF front-end components.*

*Since 2008 Dr. Ndip has also been a Lecturer in the Department of High-Frequency and Semiconductor System Technologies, School of Electrical Engineering and Computer Sciences, Technical University Berlin. He is currently engaged in teaching courses on Numerical Techniques in Electromagnetics and on Electromagnetics for Design and Integration of Microsystems. He has more than 100 publications and has won 6 best paper awards at leading international conferences. Dr. Ndip is also a recipient of the Tiburtius-Prize, awarded yearly for outstanding Ph.D. dissertations in the state of Berlin, Germany.*

**Dr. Ege Engin** *received his B.S. and M.S. degrees in electrical engineering from Middle East Technical University, Ankara, Turkey, and from University of Paderborn, Germany in 1998 and 2001, respectively. He received his Ph.D degree with Summa Cum Laude from the University of Hannover, Germany in 2004. Dr. Engin has worked as a research engineer with the Fraunhofer-Institute for Reliability and Microintegration in Berlin, Germany and at Georgia Tech. He is currently an Assistant Professor in the Electrical and Computer Engineering Department of San Diego State University. He has more than 60 publications in the areas of signal and power integrity modeling and simulation and 4 patent applications. He has co-authored the book "Power Integrity Modeling and Design for Semiconductors and Systems," published by Prentice Hall in 2007.*

**Dr. Antonio Ciccomancini Scogna** *received the Laura and Ph.D. degrees in electrical engineering from the University of L'Aquila, L'Aquila, Italy, in 2001 and 2005, respectively. He is currently a Principal Engineer at Computer Simulation Technology (CST) of America, Framingham, MA. His research interests include electromagnetic compatibility numerical modeling, printed and integrated circuits, electromagnetic packaging effects, signal integrity and power integrity analysis in high-speed digital systems. He has authored or coauthored more than 50 publications in IEEE journal transactions, IEEE conference proceedings, and Electronic Design Automation (EDA) magazines. Dr. Ciccomancini is a member of Applied Computational Electromagnetic Society (ACES), Institution of Engineering and Technology (IET), EMC TC-9 and TC-10 Committees. In 2004, he received the CST University Publication Award for the use of the finite-integration technique in signal integrity applications. He is the recipient of DesignCon Finalist Best Paper Award in 2007 and DesignCon Best Paper Award in 2008.*

**Salon Rooms 1-10**

## T7: Managing the Effects of Mechanical Stress on Performance of Modern SOCS
## PDC Instructor: Riko Radojcic, QTI Qualcomm; Valeriy Sukharev, Mentor Graphics Corporation; and Ehrenfried Zschech, Fraunhofer Institute

### Salon 1

**Course Description:** The proposed course is intended to focus on the potential issues caused by mechanical stress in modern ICs, and specifically on the potential effects of stress on device parametric characteristics. With the current technology trends towards softer insulators and harder conductors, on and off the chip, and with the continued trend towards sub-mm overall component thicknesses, the distribution of strain precipitated by the CPI-driven stress, is expected to be significantly different than in the past. In addition, new features, such as TSVs, and new integration schemes, such as SiP solutions, introduce new sources of stress. This stress results in shifts og device performance and parametric characteristics - phenomena that are harder to detect and hence harder to fix than the traditional CPI issues, such as cracks and delamination. Consequently, this new class of CPI must be addressed proactively during product design. This course will describe the major components of an eco system developed to address this problem. The course is broken into three phases:

1. Product Challenges - a discussion of the various sources of CPI stress and the trends in the technology that make the modern SoC devices susceptible to strain. This portion will also address the challenges of including stress awareness in product design.

2. Modeling Challenges - a discussion of the various modeling methodologies, and a description of techniques used in the simulation tool. This portion will also define the material parameters required.

3. Material Characterization Challenges - discussion of the various characterization techniques for multi-scale materials data, particularly stress, and the selection of the specific solutions used. This portion of the course also describes a specific study conducted to validate the entire methodology.

**Who Should Attend?** - Chip and Package Design Engineers - Product Managers - Technology Integration Engineers - Failure Analysis Engineers - Reliability Engineers

**Riko Radojcic** *is a Senior Director of Engineering at Qualcomm QTI, and a leader of 3D Technology team. Radojcic has more than thirty year's experience in the semiconductor industry; and held various positions as an independent consultant, and at PDF Solutions, Tality, Cadence, Unisys and Burroughs. Radojcic received his BSc and PhD from University of Salford, UK.*

**Valeriy Sukharev** *is a Technical Lead at the Design to Silicon Division of Mentor Graphics Corporation, Fremont, CA. Sukharev leads research and development of new full-chip modeling and simulation capabilities for the semiconductor processing and DFM/DFR applications. Prior to Mentor Graphics, Dr. Sukharev was a Visiting Professor with Brown University, Providence, RI, and a Guest Researcher with NIST, Gaithersburg, MD. He held senior technical positions at LSI Logic Advanced Development Lab, Milpitas, CA. He holds Ph.D. in physical chemistry from the Russian Academy of Sciences.*

**Ehrenfried Zschech** *is Division Director at Fraunhofer Institute for Nondestructive Testing in Dresden. His responsibilities include micro- and nanoanalysis as well as R&D in the field of test systems. He received his diploma degree in solid-state physics and his Dr. rer. nat. degree from Dresden University of Technology. Zschech gathered experience in industry, during 17 years in several technical and management positions at Airbus and AMD. He holds honorary professorships for nanomaterials at the Brandenburg University of Technology in Cottbus and for nanoanalysis at the Dresden University of Technology. Zschech is acting as President of the Federation of European Materials Societies (FEMS).*

## T8: Introduction to the Design and Fabrication of RF, High Speed and Microwave Hybrids, MCM's and Modules
## PDC Instructor: Tom Terlizzi, GM Systems LLC

### Salon 9

**Course Description:** The course presents electrical and physical design, manufacturing, materials, quality and reliability information in terms understandable to engineering and non-engineering personnel. RF Packaging history, characteristics and drivers will be outlined. Types of packages (IC, chip scale, MEMS, Hybrid, MCM, Flip Chip, BGA, Aluminum and Kovar housings) and substrates (Thick and thin film, HTCC, LTCC ceramic, organic) and critical differences among them and their High Frequency applications (Microstrip, Stripline, Coplanar will be discussed. RF and Microwave layout and the commonly used design tools and software will be outlined. The course will look at the design selection to meet use and application environments. Step-by-step manufacturing flow for different packages and products will be presented as an example to understand the complexity of processes, materials and equipment involved in their manufacture. RF & Microwave packaging concepts will be introduced and the tradeoffs of different interconnect methodology (connectors, wire bonds, ribbon bonds, AuSi & AuSn eutectic, soft solder and epoxy. Materials selection with respect to thermal resistance will be discussed. Finite Element and reliability software will be discussed to insure the design will perform to specification. Quality and reliability issues related to RF packaging and their present and future solutions will be outlined.

**Who Should Attend?** It will help the attendees to understand the application and assembly of Rf and Microwave microelectronic package technology on the next level interconnect and the service environment that microelectronic packages must protect its components. Personnel (Design engineers and process engineers) entering the RF microelectronic packaging field will have a critical look at the electrical design, physical design, layout quality, reliability and material issues related to the development and manufacture of microwave modules. Non-packaging personnel will learn the ins and outs of RF packaging. Non-technical personnel will learn the material and manufacturing intricacies of RF and Microwave microelectronic packages and the associated buzzwords used to describe them.

**Tom Terlizzi** *is VP at GM Systems, a Management and Technology consulting firm, providing Microelectronic Business & Technology plans, , Marketing & Sales strategy, Product development for microelectronic projects and business proposal support. He has designed and developed Power management systems, Single board computers, microelectronic circuits, hybrids, COB modules, ICs, RF modules, for over 30 years for military, aerospace, telecom and consumer markets as a VP/GM, Director of marketing, Chief Engineer, Operations/Engineering manager at Aeroflex, Norden/UTC, G.I. Microelectronics and Grumman. He spearheaded acquisitions of several high tech companies,ISO9000/Mil-PRF-38534 quality certifications. He received a BEE from CCNY, a MSEE from NYU-Poly & has published several articles, papers and tutorials at international conferences, edited books on electronic packaging, consulted for the DoD on advanced RF electronic packaging. Tom was the Metro ISHM Chapter President in 1983 and in his free time also writes a Blog for EDN Magazine Online - Looking @ electronics.*

Salon Rooms 1-10

# Exhibit Floorplan

## Exhibition in the GRAND BALLROOM

## Win Some $$ - Take Home One of our Great Auction Items....

Support the *Microelectronics Foundation* and the young engineers/students who benefit from this charity by participating in this year's 50/50 raffle or the silent auction.

The 50/50 raffle will take place during Monday's Welcome Reception in Junior Ballroom F. Tickets will be sold throughout the Reception and one winner will be drawn near the conclusion of the Reception. The winner takes home 50% of the total cash collected while the other 50% is donated to the Foundation.

Also be sure to take a look at the many great Silent Auction items this week, also benefitting the Foundation. We'll have fine bottles of wine, Dom Perignon Champagne, hotel vouchers, golf items, and much more. The auction will be open during the Welcome Reception, and then on display outside the exhibit hall Tuesday and Wednesday. The auction will close at 7pm on Wednesday as the Exhibit Hall Reception winds down. 100% of the money raised during the auction goes directly to the Foundation.

**Contact Brian Schieman or Dave Virissimo at registration if you have questions or wish to donate.**

# You Cannot Miss What's Happening in the Hall!

### Exhibition in the GRAND BALLROOM

The IMAPS 2013 exhibition is new and improved this year, with more companies on display, and more reasons than ever before to spend all your available time in the GRAND BALLROOM. This year, the exhibition is open two days: Tuesday, October 1 (11am-5pm) and Wednesday, October 2 (9am-7:30pm). These Conference days go quickly so take a look at the Floorplan (page 22), the Exhibit Directory (pages 24-36), the Products & Services Directory (pages 37-39) and maximize your time in the hall visiting the companies you need to speak to about new products, services, and the solutions you need. Here's a reminder about the many great reasons to spend lots of time in the GRAND BALLROOM this year…

- 126 Exhibit Booths on Display
- The latest and greatest products and services for the microelectronics/packaging supply chain on display, including new product launches from many organizations.
- Have a packaging challenge (materials, process, or others)? *The solution is likely in the hall!*
- The all NEW **"Research Lab Corridor"** featuring: Alabama Microelectronics Science & Technology Center; Center for Nanoscale Science & Eng., North Dakota State University; Desich SMART Center; Fraunhofer IKTS; Fraunhofer IZM; and Georgia Tech 3D Systems Packaging Research Center (PRC).
- Need a jolt of caffeine?! Take your refreshment breaks at ***IMAPS Cafés*** in the hall:

  IMAPS Cafés Sponsored by:

- Grab a delicious treat during the all new ***Dessert "Happy Hour"*** Tuesday from 3:15-4:30pm:

  Dessert "Happy Hour" Sponsored in Part by:

- ***Wednesday's Lunch is on us!*** Bring your lunch ticket and grab a sandwich from 12:15-1:30pm:

  Wednesday's Exhibit Hall Lunch Sponsored In Part by:

- The exhibit closes with some fun! Join the ***Exhibit Hall Reception*** Wednesday, 5:30-7:30pm:

  Exhibit Hall Reception sponsored by:

- Need to e-mail or to get on-line? Visit the ***Internet Café*** or access the ***wireless internet*** ONLY in the hall:

  Internet Café and Wireless Internet Sponsored by:

- The ***Student Poster Session***
- Exhibitor give-aways and exciting ***Raffles!***

**3D Plus USA • Booth # 201**
6633 Eldorado Pkwy., # 420, McKinney, TX 75070 USA
(P) 214-733-8505
(E) memond@3d-plususa.com
(W) www.3d-plususa.com

3D Plus is a worldwide supplier of advanced high density 3D microelectronic products and Die Stacking technologies meeting the demand for high reliability, high performance and very small size of today's and tomorrow's electronics.

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**ACM Research, Inc. • Booth # 421**
42307 Osgood Rd., Fremont, CA 94539 USA
(P) 510-445-3700
(E) michael.lee@acmrcsh.com
(W) www.acmrcsh.com

ACM Research, Inc. was founded in 1998 in Silicon Valley. In September 2006, ACM shifted its focus to Asia, forming ACM Shanghai subsidiary. The company is now located in Shanghai's Zhangjiang High-Tech Park. In where, it conducts research, development, engineering, manufacturing, marketing, sales and service activities. ACM specializes in wet process equipment including single-wafer megasonic cleaning tools (Ultra C), copper stress free polishing (Ultra SFP) and copper plating (Ultra ECP).

ACM has a strong IP portfolio with over 100 patents filed internationally. ACM is committed to providing customers with advanced technology solutions, low cost of owner –ship, world-class products, service and engineering.

**AdTech Ceramics • Booth # 800**
511 Manufacturers Road, Chattanooga, TN 37405 USA
(P) 423-488-1184
(E) brian.bukovitz@adtechceramics.com
(W) www.adtechceramics.com

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100 Flagship Drive, North Andover, MA 01845 USA
(P) 978-552-1221
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(W) www.advancerepro.com

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YINCAE Advanced Materials, LLC is a developer, manufacturer and supplier of high performance coatings, adhesives, electronic and optoelectronic materials. YINCAE products are mainly involved in: solder joint encapsulant, underfill materials, board-level assembly materials, die attach adhesives, optical adhesives, nanofilm, anti-warpage materials, thermal interface materials and conformal coatings.

**Zeon Corporation • Booth # 419**
4111 Bells Lane, Louisville, KY 40211 USA
(P) 502-775-2027
(E) shoulders@zeonchemicals.com
(W) www.zeonchemicals.com

Zeon Corporation/Zeon Chemicals L.P., USA have developed two innovative state-of-the-art packaging materials: 1) “Ultra-Low Loss Build-Up Film” for high speed IC packages and WLP requiring superior electrical properties, and 2) “Ultra-Low Loss PCB Materials” for high speed servers and RF/mobile applications for technology leading devices.

# Products and Services Directory

### 3D IC and Packaging Technologies, TSV, TGV

| Company | BOOTH # |
|---|---|
| CVInc. | 317 |
| Endicott Interconnect Technologies | 200 |
| ENrG Incorporated | 215 |
| Fraunhofer IZM | 426 |
| Georgia Tech PRC | 726 |
| IBM | 418 |
| Interconnect Systems, Inc. | 406 |
| Neu Dynamics Corporation | 712 |
| nScrypt Inc. | 716 |
| Palomar Technologies, Inc. | 511 |
| Plasma-Therm, LLC | 111 |
| Quik-Pak | 518 |
| Rudolph Technologies, Inc. | 519 |
| Sonoscan, Inc. | 709 |
| Towa Corporation | 312 |
| YINCAE Advanced Materials | 818 |

### Assembly Equipment-tools, fixtures, dispensing & rework equipment

| Company | BOOTH # |
|---|---|
| ATV Technologie GmbH. | 322 |
| CVInc. | 317 |
| Finetech | 508 |
| Georgia Tech PRC | 726 |
| Kulicke & Soffa Industries Inc. | 705 |
| Midas Technology, Inc. | 803 |
| Neu Dynamics Corporation | 712 |
| nScrypt Inc. | 716 |
| Palomar Technologies, Inc. | 511 |
| Perfection Products, Inc. | 515 |
| Semiconductor Equipment Corporation | 410 |
| TDK Corporation | 804 |
| Towa Corporation | 312 |
| Trebor Instrument Corp. | 404 |
| Tresky Corporation | 708 |
| UTZ Technologies | 817 |

### Bonding Equipment-tools, pull testers, & bonding wire

| Company | BOOTH # |
|---|---|
| ATV Technologie GmbH. | 322 |
| Coining, Inc., an Ametek Company | 614 |
| Deweyl Tool Company | 316 |
| F&K Delvotec | 405 |
| Finetech | 508 |
| Georgia Tech PRC | 726 |
| Hesse Mechatronics, Inc. | 605 |
| Kulicke & Soffa Industries Inc. | 705 |
| Neu Dynamics Corporation | 712 |
| Nordson DAGE | 701 |
| Palomar Technologies, Inc. | 511 |
| Perfection Products, Inc. | 515 |
| The Prince & Izant Companies | 105 |
| Royce Instruments, Inc. | 516 |
| Semiconductor Equipment Corporation | 410 |
| TDK Corporation | 804 |
| Trebor Instrument Corp. | 404 |
| Tresky Corporation | 708 |
| XYZTEC | 423 |

### Chemicals and Gases – photochemicals

| Company | BOOTH # |
|---|---|
| Metalor Technologies USA | 807 |
| Technic Inc | 205 |

### Cleaning equipment, not including chemicals

| Company | BOOTH # |
|---|---|
| ATV Technologie GmbH. | 322 |
| BSET EQ | 322 |
| Geib Refining Corp. | 609 |
| Neu Dynamics Corporation | 712 |

### Computer Design, CAD/CAM-design services

| Company | BOOTH # |
|---|---|
| Infinite Graphics | 206 |
| Neu Dynamics Corporation | 712 |
| NOVA Integration Solutions, Inc. (NIS) | 323 |
| The Prince & Izant Companies | 105 |
| UTZ Technologies | 817 |

### Connectors, lead forming and frames

| Company | BOOTH # |
|---|---|
| Interconnect Systems, Inc. | 406 |
| Neu Dynamics Corporation | 712 |
| NOVA Integration Solutions, Inc. (NIS) | 323 |
| Photofabrication Engineering, Inc. (PEI) | 318 |
| The Prince & Izant Companies | 105 |
| Souriau PA&E | 610 |
| Trebor Instrument Corp. | 404 |

### Dicing & Die attachment equipment

| Company | BOOTH # |
|---|---|
| ATV Technologie GmbH. | 322 |
| Finetech | 508 |
| Neu Dynamics Corporation | 712 |
| Perfection Products, Inc. | 515 |
| Plasma-Therm, LLC | 111 |
| Semiconductor Equipment Corporation | 410 |
| Towa Corporation | 312 |
| Trebor Instrument Corp. | 404 |

### Electronic Packages & Packaging

| Company | BOOTH # |
|---|---|
| AdTech Ceramics | 800 |
| AI Technology, Inc. | 400 |
| ATV Technologie GmbH. | 322 |
| Center for Nanoscale Science & Eng., North Dakota State University | 327 |
| CeramTec GmbH | 307 |
| Coining, Inc., an Ametek Company | 614 |
| Colorado Microcircuits Inc. | 315 |
| Conductive Containers Inc. | 313 |
| CVInc. | 317 |
| DuPont Microcircuit Materials | 520 |
| Endicott Interconnect Technologies | 200 |
| Fraunhofer Institute for Ceramic Technologies and Systems IKTS | 526 |
| Fraunhofer IZM | 426 |
| Georgia Tech PRC | 726 |
| IBM | 418 |
| Metalor Technologies USA | 807 |
| Micross Components | 721 |
| Natel Electronic Manufacturing Services | 505 |
| Neu Dynamics Corporation | 712 |
| NorCom Systems, Inc. | 613 |
| NOVA Integration Solutions, Inc. (NIS) | 323 |
| nScrypt Inc. | 716 |
| NTK Technologies | 719 |
| Palomar Technologies, Inc. | 511 |
| Photofabrication Engineering, Inc. (PEI) | 318 |
| Quik-Pak | 518 |
| Souriau PA&E | 610 |
| Torrey Hills Technologies, LLC | 408 |
| Towa Corporation | 312 |
| UTZ Technologies | 817 |
| YINCAE Advanced Materials | 818 |

### Electronic Microscopy Services, analytical services

| Company | BOOTH # |
|---|---|
| Center for Nanoscale Science & Eng., North Dakota State University | 327 |
| Fraunhofer IZM | 426 |
| Georgia Tech PRC | 726 |
| Hi-Rel Laboratories | 612 |
| Oneida Research Services, Inc. | 422 |
| Sonoscan, Inc. | 709 |

### Environmental Control-clean rooms

| Company | BOOTH # |
|---|---|
| Conductive Containers Inc. | 313 |
| Georgia Tech PRC | 726 |

### Epoxies & Adhesives

| Company | BOOTH # |
|---|---|
| AI Technology, Inc. | 400 |
| Coining, Inc., an Ametek Company | 614 |
| Indium Corporation | 409 |
| LORD Corporation | 600 |
| NAMICS Corporation | 611 |
| Polysciences, Inc. | 620 |

### Failure Analysis

| Company | BOOTH # |
|---|---|
| ATV Technologie GmbH. | 322 |
| BSET EQ | 322 |
| Center for Nanoscale Science & Eng., North Dakota State University | 327 |
| Endicott Interconnect Technologies | 200 |
| Fraunhofer IZM | 426 |
| Hi-Rel Laboratories | 612 |
| IBM | 418 |
| Nordson DAGE | 701 |
| Oneida Research Services, Inc. | 422 |
| The Prince & Izant Companies | 105 |
| Sonoscan, Inc. | 709 |

### Furnace Equipment-materials handling

| Company | BOOTH # |
|---|---|
| ATV Technologie GmbH. | 322 |
| Harrop Industries, Inc. | 714 |
| The Prince & Izant Companies | 105 |
| Torrey Hills Technologies, LLC | 408 |

# Products and Services Directory

### Hybrid/SMT – Manufacturing circuit boards and flex circuit manufacturing

| Company | BOOTH # |
|---|---|
| BSET EQ | 322 |
| DuPont Microcircuit Materials | 520 |
| Endicott Interconnect Technologies | 200 |
| Fraunhofer IZM | 426 |
| Micro Hybrid Dimensions, Inc. | 414 |
| Natel Electronic Manufacturing Services | 505 |
| Palomar Technologies, Inc. | 511 |
| Photofabrication Engineering, Inc. (PEI) | 318 |
| UTZ Technologies | 817 |
| YINCAE Advanced Materials | 818 |

### Inspection Equipment and Services

| Company | BOOTH # |
|---|---|
| BSET EQ | 322 |
| Center for Nanoscale Science & Eng., North Dakota State University | 327 |
| Hi-Rel Laboratories | 612 |
| Infinite Graphics | 206 |
| Neu Dynamics Corporation | 712 |
| NorCom Systems, Inc. | 613 |
| Nordson DAGE | 701 |
| Oneida Research Services, Inc. | 422 |
| Palomar Technologies, Inc. | 511 |
| The Prince & Izant Companies | 105 |
| Rudolph Technologies, Inc. | 519 |
| Sonoscan, Inc. | 709 |
| Trebor Instrument Corp. | 404 |

### Lasers-cutting, scribing, trimming, marking, machining, welding & supplies

| Company | BOOTH # |
|---|---|
| Center for Nanoscale Science & Eng., North Dakota State University | 327 |
| CeramTec GmbH | 307 |
| Neu Dynamics Corporation | 712 |
| Perfection Products, Inc. | 515 |
| The Prince & Izant Companies | 105 |
| Souriau PA&E | 610 |

### Machining-trimming and scribing non-laser

| Company | BOOTH # |
|---|---|
| CeramTec GmbH | 307 |
| Neu Dynamics Corporation | 712 |
| NOVA Integration Solutions, Inc. (NIS) | 323 |
| The Prince & Izant Companies | 105 |
| Souriau PA&E | 610 |
| Stellar Industries Corp. | 401 |

### Reflow Equipment

| Company | BOOTH # |
|---|---|
| ATV Technologie GmbH | 322 |
| BSET EQ | 322 |
| Midas Technology, Inc. | 803 |
| Palomar Technologies, Inc. | 511 |
| Sikama International, Inc. | 816 |
| Torrey Hills Technologies, LLC | 408 |
| Tresky Corporation | 708 |

### Solder-pastes & creams

| Company | BOOTH # |
|---|---|
| Indium Corporation | 409 |
| The Prince & Izant Companies | 105 |

### Screen Printers, Screens & Stencils

| Company | BOOTH # |
|---|---|
| Geib Refining Corp. | 609 |
| Hary Manufacturing Inc. (HMI) | 500 |
| Infinite Graphics | 206 |
| MicroScreen, LLC | 523 |
| Riv, Inc. | 700 |
| Sefar, Inc. | 204 |

### Semiconductors-distributors & manufacturers

| Company | BOOTH # |
|---|---|
| Advanced Dicing Technologies, Inc. | 517 |
| BSET EQ | 322 |
| Conductive Containers Inc. | 313 |
| Indium Corporation | 409 |
| Interconnect Systems, Inc. | 406 |
| Micross Components | 721 |
| Minco Technology Labs, LLC. | 309 |
| Palomar Technologies, Inc. | 511 |
| The Prince & Izant Companies | 105 |
| SemiDice, Inc. | 707 |

### Substrates-shapes

| Company | BOOTH # |
|---|---|
| AdTech Ceramics | 800 |
| CeramTec GmbH | 307 |
| ENrG Incorporated | 215 |
| Georgia Tech PRC | 726 |
| Infinite Graphics | 206 |
| Natel Electronic Manufacturing Services | 505 |
| NTK Technologies | 719 |
| The Prince & Izant Companies | 105 |
| Stellar Industries Corp. | 401 |

### Surface Mount/Hybrid Components

| Company | BOOTH # |
|---|---|
| Conductive Containers Inc. | 313 |
| Fraunhofer IZM | 426 |
| Palomar Technologies, Inc. | 511 |
| Photofabrication Engineering, Inc. (PEI) | 318 |
| Technic Inc | 205 |
| Torrey Hills Technologies, LLC. | 408 |
| UTZ Technologies | 817 |

### Thick and/or Thin Film Materials-precious metals & polymers

| Company | BOOTH # |
|---|---|
| AI Technology, Inc. | 400 |
| Ceradyne VIOX, Inc., a 3M company | 717 |
| DuPont Microcircuit Materials | 520 |
| ESL ElectroScience | 808 |
| Ferro Corporation | 615 |
| Geib Refining Corp. | 609 |
| Georgia Tech PRC | 726 |
| Heraeus Thick Film Division | 504 |
| Indium Corporation | 409 |
| LORD Corporation | 600 |
| Metalor Technologies USA | 807 |
| The Prince & Izant Companies | 105 |
| Technic Inc | 205 |
| UTZ Technologies | 817 |
| YINCAE Advanced Materials | 818 |

### Test Equipment-probes, probe cards & die sorting equipment

| Company | BOOTH # |
|---|---|
| BSET EQ | 322 |
| Georgia Tech PRC | 726 |
| Neu Dynamics Corporation | 712 |
| NorCom Systems, Inc. | 613 |
| NTK Technologies | 719 |
| Royce Instruments, Inc. | 516 |
| Rudolph Technologies, Inc. | 519 |
| Sonoscan, Inc. | 709 |
| Trebor Instrument Corp. | 404 |

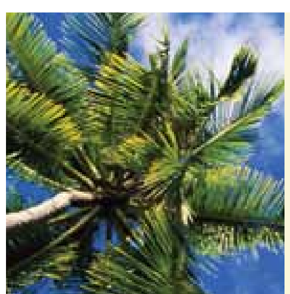
### Industry Publications

| Company | BOOTH # |
|---|---|
| U.S. TECH. | 806 |

# Products and Services Directory

## Other Products/Services

| Company Name | Booth # | Description |
|---|---|---|
| AI Technology, Inc. | 400 | Thermal Products |
| ancosys Inc. | 805 | Wet chemical process monitoring and control |
| Beijing Tian-Long Tungsten & Molybdenum Co., Ltd. | 213 | Tungsten Copper heat sinks, Molybdenum Copper heat sinks, Cu/Mo/Cu(CMC), Cu/MoCU/Cu(CPC), Tugnsten, Molybdenum and alloys. |
| CeramTec GmbH | 307 | Alumina/Aluminum Nitride/ZTA Ceramics. Includes substrates, heatsinks, resistor cores, inductor cores, liquid cooled technologies. Lasering, metallizing, extrusion, dry pressing, lapping. |
| Coining, Inc., an Ametek Company | 614 | Tape & Reel Packaging |
| Desich SMART Center | 626 | MEMS package, assembly, and test development services |
| ENrG Incorporated | 215 | Ultrathin flexible ceramic substrates and membranes. |
| Fraunhofer Institute for Ceramic Technologies and Systems IKTS | 526 | Smart Microsystems Thick film pastes Multilayer LTCC HTCC |
| Geib Refining Corp. | 609 | precious metal materials, refining, and reclaim |
| General Metal Finishing | 310 | Specification plating and electropolishing services |
| Harrop Industries, Inc. | 714 | Tape casting machines |
| Hary Manufacturing Inc. (HMI) | 500 | Substrate handling / automation equipment Infra Red conveyor dryers |
| Hesse Mechatronics, Inc. | 605 | thin wire wedge bonders, heavy wire wedge bonders, ribbon bonders |
| Hi-Rel Laboratories | 612 | Destructive Physical Analysis (DPA), Materials Analysis, Real-time X-ray, CSAM, FTIR, SEM/EDS, cross sectional analysis, Dye & Pry testing, Prohibited Materials Analysis (testing for pure tin surfaces), Construction analysis, PIND, Hermeticity |
| IBM | 418 | Packaging Joint Development Ecosystem |
| Infinite Graphics | 206 | Photomasks, 3D structures |
| Micross Components | 721 | Component Modification, including solder exchange, reballing and lead attach. |
| NAMICS Corporation | 611 | Underfills NCP NCF Dam and fill Non-conductive films Solar electrode paste |
| Natel Electronic Manufacturing Services | 505 | Custom microelectronics assembly, LTCC and ALN substrates & packages, Thick Film and Thin Film Mil-Std 38534 H and K qualified |
| NOVA Integration Solutions, Inc. (NIS) | 323 | Enclosure & chassis thermal and structural analysis. |
| Pacific Trinetics Corporation, Inc. | 621 | Manufacturer of Punch, Via Filler, Screen Printer, Stacker, Laminator & Cutting Equipments |
| Palomar Technologies, Inc. | 511 | Contract Manufacturing Wire Bond & Die Attach Training Process Development Consulting |
| Photofabrication Engineering, Inc. (PEI) | 318 | PEI specializes in etching custom products from base materials such as kovar, nickel, stainless steel, cold rolled steel, and titanium, with selective plating and other finishes. |
| Polysciences, Inc. | 620 | Custom Formulation of Adhesives, Coatings and Encapsulants |
| The Prince & Izant Companies | 105 | Metal Reclamation Manufacturing Stocking & Kitting Programs Technical Support |
| Reldan Metals Co div of Abington Reldan Metals ,LLC | 305 | Refiner Precious Metals |
| Rudolph Technologies, Inc. | 519 | Process control software, Yield management software, advanced packaging lithography |
| SemiDice, Inc. | 707 | Bare Die Distributor and Wafer Processing Services. Both active and passive lines include: Analog Device, Fairchild Semiconductor, Texas Instruments, Microsemi Corp, Cree Inc, International Rectifier, Vishay Intertechnology, ON Semiconductor, NXP, ISSI, Central Semi, IRC Advanced Fil, Johanson Dielectrics, Novacap Vishay Electrofilms, Value-added services include testing; electrical probing, LAT's, Burn-in, Class H, K. Hi Rel division and extensive inventory with a broad product mix available. |
| Souriau PA&E | 610 | EMI filters |
| Stellar Industries Corp. | 401 | Thin Film Substrates, Thick Film Substrates, DBCu Substrates |
| Technic Inc | 205 | Mazerustar Planetary Mixers |
| Towa Corporation | 312 | Package Singulation |
| Trebor Instrument Corp. | 404 | Machine Shop Service, Delidding Service. |



# Symposium Committee

| Position | Name | Affiliation |
|---|---|---|
| General Chair | Matt Nowak | Qualcomm, Inc. |
| Technical Chair | Ivan Ndip | Fraunhofer IZM |
| Technical Co-Chair, USA | Mark Hoffmeyer | IBM Corporation |
| Technical Co-Chair, Europe | Andre Rouzaud | CEA LETI |
| Technical Co-Chair, Asia | Jin Yu | Korea Advanced Institute of Science and Technology (KAIST) |
| Assistant Technical Co-Chair, USA | Erica Folk | Northrop Grumman |
| Assistant Technical Co-Chair, Europe | Gilles Poupon | CEA LETI |
| Assistant Technical Co-Chair, Asia | Woong-Sun Lee | SK Hynix |
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| Student Activities Co-Chair | Tom Weller | University of South Florida |
| Student Activities Co-Chair | Ege Engin | San Diego State University |
| Student Activities Co-Chair | Mike Newton | Newton Cyberfacturing |
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| GBC Co-Chair | Lee Smith | Plexus Corp. |
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| Foundation High School Chair | Mike Newton | Newton Cyberfacturing |
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| Exhibits Chair | Greg Caswell | DfR Solutions |

**Additional Leadership and Staff:**

| Position | Name | Affiliation |
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| IMAPS Membership & Events Coordinator | Brianne Lamm | IMAPS |

# Technical Program At-a-Glance

## Tuesday, October 1, 2013

**8:00 AM—11:15 AM**

| INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|
| **TSV Materials & Processes** *Chairs: Gabriel Pares, CEA; Sesh Ramaswami, Applied Materials* | **Design & Analysis for Reliability** *Chairs: Stevan Hunter, ON Semiconductor; Gopal Jha, Avago Technologies* | **Advanced Materials & Novel Assembly Processes** *Chairs: Erica Folk, Northrop Grumman; Yoon-Chul Sohn, Samsung Advanced Institute of Technology* | **Pb-Free Solder & ROHS** *Chairs: John Bolger, Department of Defense; John Pan, Cal Poly State University* | **Medical Device Packaging** *Chairs: Sean Ferrian, Ferrian Sales & Associates; Ying Yu, IBM* | **European Perspective on Packaging Trends** *Chairs: Andre Rouzaud, CEA LETI; Martin Schneider-Ramelow, Fraunhofer IZM* |

**2:00 PM—6:35 PM**

| INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|
| **Advanced Platform Integration** *Chairs: Urmi Ray, Qualcomm; Kyu-oh Lee, Intel* | **Modeling and Design for SI and Reliability** *Chairs: Chris Pan, Qualcomm; Judy Priest, Cisco* | **Polymers, Underfill, Encapsulants and Adhesives** *Chairs: Jeff Gotro,Innocentrix; Lyndon Larson, Dow Corning* | **Wirebonding & Stud Bumping** *Chairs: Dan Evans, Palomar Technologies; Lee Levine, Process Solutions Consulting* | **Emerging Technologies** *Chairs: Susan Bagen, Endicott Interconnect; Igor Prikhodko, Analog Devices* | **Asian Perspective on Electronic Packaging and System Integration** *Chairs: Tae-Kyu Lee, Cisco; Woongsun Lee, SK Hynix* |

## Wednesday, October 2, 2013

**8:00 AM—11:15 AM**

| INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|
| **Packaging Transitions: 2.5D and 3D Interconnect Technologies from Wire Bond to RDL to TSV** *Chairs: Greg Caswell, DfR Solutions; Cristina Chu, TEL NEXX* | **Thermal and Thermo-Mechanical Modeling** *Chairs: David Saums, DS&A LLC; Mary Cristina Ruales Ortega, University System Ana G. Mendez* | **Substrate Materials I** *Chairs: Michael Folk, Northrop Grumman Corp.; Jeff Hartman, Northrop Grumman Corp.* | **Flip Chip Bumping** *Chairs: Andy Strandjord, Pac Tech USA; Nick Renaud-Bezot, AT&S* | **New Concepts, Interconnects & Processes for High Performance Packaging** *Chairs: Benson Chan, Endicott Interconnect; Ron Lasky, Indium Corporation* | **Power Packaging I** *Chairs: Mark Hoffmeyer, IBM Corporation; Doug Hopkins, North Carolina State University* |

**2:00 PM—5:30 PM**

| INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|
| **Glass Interposers** *Chairs: Steve Annas, Triton Micro Tech; Aric Shorey, Corning Inc.* | **Testing Methods and Process for Improved Reliability** *Chairs: Mike Ferrara, RF Micro Devices; Akhlaq Rahman, Thin Film Corp.* | **Substrate Materials II (Ceramic & LTCC)** *Chairs: Dan Krueger, Honeywell FM&T; Ken Peterson, Sandia National Labs.* | **MEMS & Sensor Packaging** *Chairs: Matt Apanius, SMART Commercialization Center for Microsystems; Ron Jensen, Honeywell* | **Think Thin: Thin IC Packaging For Mobile Devices** *Chairs: Rich Rice, ASE; Jason Cho, ASE; Milind Shah, Qualcomm* | **Power Packaging II** *Chairs: Julie Adams, UBOTIC Company Ltd.; Mark Hoffmeyer, IBM Corporation* |

## Thursday, October 3, 2013

**1:00 PM—5:00 PM**

| INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|
| **Technologies and Methods for 2.5/3D Packaging and Integration** *Chairs: Anwar Mohammed, John Hunt, ASE US* | **RF and Microwave Packaging** *Chairs: Xiaoguang "Leo" Liu, University of California, Davis; Fred Barlow, University of Idaho* | **Bonding Materials and Processes** *Chairs: Maria Durham, Indium Corporation; Klaus-Dieter Lang, Fraunhofer IZM* | **LED and Optoelectronics Packaging** *Chairs: Tolga Tekin, Fraunhofer IZM; Luu Nguyen, Texas Instruments* | **Printed Electronics & Additive Manufacturing** *Chairs: Mike Newton, Newton Cyberfacturing; Yiliang Wu, Xerox Research Centre of Canada* | **Electronic Packaging for Harsh Environment Applications** *Chairs: Aicha Elshabini, University of Idaho; Tom Buschor, Harris Corporatio* |

## Keynotes and Panel Discussion

**Tuesday • 12:00 PM – 12:45 PM — Junior Ballroom F**

**KEYNOTE: Next Generation of Electronic Systems - Challenges and Solutions for System Integration Technologies**

Prof. Dr. -Ing. Dr. sc. techn. Klaus-Dieter Lang - Klaus-Dieter Lang, Professor, School of Electrical Engineering and Computer Sciences at the Technical University Berlin, Germany

**Wednesday • 11:20 AM – 12:05 PM — Junior Ballroom F**

**KEYNOTE: Progress in Developing an Open Supply Chain for 2.5D/3D Market Enablement**

David McCann, Vice President of Packaging, GLOBALFOUNDRIES, Malta, New York

**Wednesday • 12:30 PM – 2:00 PM — Junior Ballroom G**

**GLOBAL BUSINESS COUNCIL (GBC) Keynote Luncheon & Market Forecasting Analyst Session**

Claudius Feger, IBM Research – Brazil, feger@us.ibm.com

**Thursday • 8:00 AM –12:00 PM — Junior Ballroom F**

**An entire morning of the conference dedicated to 2.5D & 3D IC, Interposers, Packaging**

# Technical Program

## Tuesday, October 1, 2013 — Salon Rooms 1-6

| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| 8:00 AM –11:15 AM | **TSV Materials & Processes**<br>*Chairs: Gabriel Pares, CEA; Sesh Ramaswami, Applied Materials*<br>TSV is one of the key technologies for 3D. Significant improvements have already been achieved on the materials and processes involved for its fabrication. However there still a lot to do to make it reliable and ready for high volume production. | **Design & Analysis for Reliability**<br>*Chairs: Stevan Hunter, ON Semiconductor; Gopal Jha, Avago Technologies*<br>High reliability is increasingly expected in microelectronic products. This session examines a variety of methods for improving device, assembly and packaging reliability by design. | **Advanced Materials & Novel Assembly Processes**<br>*Chairs: Erica Folk, Northrop Grumman; Yoon-Chul Sohn, Samsung Advanced Institute of Technology*<br>Novel packaging materials will be introduced in conjunction with packaging assembly technologies. Various organic, inorganic and metallic materials are selected for the applications of 3D integration, packaging assembly, and die attachment. | **Pb-Free Solder & ROHS**<br>*Chairs: John Bolger, Department of Defense; John Pan, Cal Poly State University*<br>The continuing challenges of implementing lead-free solder will be examined in this session, as industry continues to evaluate options to improve the reliability of lead-free solder joints. | **Medical Device Packaging**<br>*Chairs: Sean Ferrian, Ferrian Sales & Associates; Ying Yu, IBM Systems & Technology Group*<br>This session will highlight materials, processes, and characterization methods for packaging biomedical devices and microfluidics to enable novel diagnostics and treatments. | **European Perspective on Packaging Trends**<br>*Chairs: Andre Rouzaud, CEA LETI; Martin Schneider-Ramelow, Fraunhofer IZM*<br>From key enabling technologies to advanced SiP and hybrid system integration: This session will give an insight on different novel technologies and materials required to fullfil the promise for the next generation of future systems. |
| 8:00 AM –8:25 AM | **FEATURED SPEAKER:**<br>Alternative technology concepts for low-cost and high-speed 2D and 3D interconnect manufacturing<br>*Fred Roozeboom, Eindhoven Univ of Technology (M. Smets, B. Kniknie, M. Hoppenbrouwers, TNO; G. Dingemans, W. Keuning, W.M.M. Kessels, Eindhoven University of Technology; R. Pohl, A.J. Huis in't Veld, University of Twente)* | Using Physics of Failure to Predict System Level Reliability for Avionic Electronics<br>*Greg Caswell, DfR Solutions* | Development of Laser and Photo-Definable Toughened Benzocyclobutene Dielectric Materials for 3D-TSV Integration<br>*Zidong Wang, Dow Electronic Materials (Greg Prokopowicz, Kevin Wang, Joe Lachowski, Zhifeng Bai, Ray Thibault, Eric Huenger, Scott Kisting, Chris Tucker, Matt Bishop, Lynne Mills, Dave Louks, Michael Gallagher)* | Effects of Minor Alloying Additive on the Shear Strength of Sn-58Bi Solder Joint<br>*Omid Mokhtari, Joining and Welding Research Institute, Osaka University (Hiroshi Nishikawa)* | **FEATURED SPEAKER**<br>How are CCD, CMOS AND A-SI Reshaping the Medical Imaging Industry?<br>*Christophe Fitamant, Yole Developpment* | **FEATURED SPEAKER**<br>Assembly and Packaging Enabling System Integration<br>*Klaus Pressel, Infineon Technologies* |
| 8:25 AM –8:50 AM | Optimizing TSV Liner Step Coverage<br>*Vijayalakshmi Seshachalam, GLOBALFOUNDRIES Inc. (Akshey Sehgal, Sarasvathi Thangaraju, Daniel Smith, Ramakanth Alapati)* | Solder Joint Reliability Study of Wafer Level Packages on Flexible Board<br>*Gary Gu, RF Micro Devices Inc (Daniel Jin, Jon Chadwick)* | Small-chip Attachment on Copper Leadframe with Sintered Nanosilver Paste<br>*Jesus Calata, Virginia Tech (Hanguang Zheng, Guo-Quan Lu, Khai Ngo, Luu Nguyen)* | Effects of Sb and Zn Addition on Impact Resistance Improvement of Sn-Bi Solder Joints<br>*Keishiro Okamoto, Fujitsu Laboratories Ltd. (Toshiya Akamatsu, Seiki Sakuyama, Keisuke Uenishi)* | Biomedical Sensor Packaging Failures: Regulations are not Design Standards<br>*Colin Drummond, Case Western Reserve University* | Smart Power Module Molding Advances: Evaluating High Temperature Suitability of Molding Compounds<br>*Karl-F. Becker, Fraunhofer IZM (T. Thomas, J. Bauer, L.-H. Daus, R. Kahle, T. Braun, R. Aschenbrenner, M. Schneider-Ramelow, K.-D. Lang)* |

# Tuesday, October 1, 2013 — Salon Rooms 1-6

| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| 8:50 AM –9:15 AM | Monitoring of Wet Etch for Wafer Thinning and Via Reveal process *Eugene Shalyt, ECI Techology (Chuannan Bai, Guang Liang, Peter Bratin)* | Ag-Wire and Ag Alloy Wire Relaibility and Molding Compound *Aya Mizushima, Hitachi chemical (Yoshinori Endo, Hidenori Abe, Shinichiro Kato, Kazuhiro Ikemura, Naoki Sadayori)* | Influence of the organic vehicle and inorganic additives on the properties of thick film pastes for AIN *Richard Schmidt, Fraunhofer IKTS (Marco Wenzel, Kathrin Reinhardt, Markus Eberstein, Lars Rebenklau)* | Effect of Fe Content on the Interfacial Reliability of SnAgCu/Fe-Ni Solder Joint *Zhi-Quan Liu, Institute of Metal Research, Chinese Academy of Sciences (Hao Zhang, Li Zhang, Hongyan Guo, Chi-Ming Lai)* | Evaluation of Epoxy Flux for Use in Hearing Aid SMD Assemblies *Susie Krzmarzick, Starkey Hearing Technologies (John Dzarnoski)* | Ultrasonically Enabled Low Temperature Electroless Plating for Advanced Electronic Manufacture *Dr Andrew J Cobley, Coventry University (Graves J E, Kassim A, Mkhlef B, Abbas B)* |
| 9:15 AM – 9:40 AM | 2.5 / 3D Packaging Technology Solution for High Frequency Device *Yasuhiro Morikawa, ULVAC,Inc. (T. Murayama1, A. Suzuki, T. Sakuishi, Y. Nakamuta and K. Suu)* | Moisture Reliability Improvement of a High Performance Depletion Mode 0.15 um Gate PHEMT Process *J. K. Abrokwah, Avago Technologies (John Stanback, Molly Johnson, Chi L. Jiaa)* | Better, Faster and Cheaper Precision Cleaning: Advanced CO2 Cleaning Technology *David Jackson, CleanLogix LLC* | Effect of ENEPIG Surface Finish on the Vibration Reliability of Solder Interconnects *Sandeep Menon, CALCE, University of Maryland (Adam Pearl, Michael Osterman, Michael Pecht)* | Anti-Counterfeit, Advanced Microelectronics Packaging Solutions for Miniaturized Medical Devices *Rabindra Das, Endicott Interconnect Technologies, Inc. (Frank D. Egitto, How Lin)* | Hybrid In-Mould Integration *Teemu Alajoki, VTT (Matti Koponen, Arttu Huttunen, Markus Tuomikoski, Mikko Heikkinen, Antti Keranen, Kimmo Keranen, Jukka-Tapani Makinen, Tuomo Jaakola, Janne Aikio, Kari Ronka)* |
| **COFFEE BREAK IN FOYER: 9:40 AM – 10:00 AM — sponsored by LORD AskUsHow™** | | | | | | |
| 10:00 AM –10:25 AM | Application of Low-K Liner for Stress and Capacitance Control in Cu-TSV *Chuan Seng Tan, Nanyang Technological University (Lin Zhang, Hongyu Li, WooSik Yoo)* | LORD SolderBraceTM for improved reliability and throughput in WLCSP *George Sears, LORD Corporation* | Copper Wirebond Compatibility with Organic and Inorganic Ions Present in Mold Compounds *Varughese Mathew, Freescale Semiconductor, Inc. (Sheila Chopin, Leo Higgins, Yingrui Zhang)* | Thermal Cycling Reliability of Alternative Low-Silver Tin-based Solders *Elviz George, CALCE, University of Maryland (Michael Osterman, Michael Pecht, Richard Coyle, Richard Parker, Elizabeth Benedetto)* | Non-hermetic Micropackage for Chronic Implantable MEMS Systems *Wen H. Ko, Case Western Reserve Univerasity (Peng Wang, Shem Lachhman, Di Sun, and C. Zorman)* | Excimer Laser Machining of Fired LTCC for Selectively Metalized Open Micro-channel Structures *Dilshani Rathnayake-Arachchige, Loughborough University (Paul Conway, David Hutt)* |
| 10:25 AM –10:50 AM | Electrografted insulator layer as copper diffusion barrier for TSV interposers *Vincent Mevellec, Alchimer (F. Raynal, D. Suhr, T. Dequivre, L. Religieux)* | Moisture and Hydrogen Release in Optoelectronics Hermetic Packages *Marwan Albarghouti, Semtech (Nayla ElDahdah, Goran Perosevic, Swati Jain)* | A non-TSV 1000+ IO Package on Package Solution for wide IO applications *Laura Mirkarimi, Invensas Corp (Rajesh Katkar, Ron Zhang, Rey Co, Zhijun Zhao)* | Voiding and Reliability of Assembly of BGA with SAC and 57Bi42Sn1Ag Alloys *Ning-Cheng Lee, Indium Corporation (Yan Liu)* | | An Overview of Isotropic Conductive Adhesives Filled with Metal-coated Polymer Spheres *Hoang-Vu Nguyen, IMST, Vestfold University College (Knut E. Aasmundtveit , IMST, Vestfold University College; Helge Kristiansen, Conpart AS; Susanne Helland, Tore Helland, Mosaic Solutions AS)* |
| 10:50 AM –11:15 AM | Analysis of Strain/Stress in Electroless Copper Films *Tobias Bernhard, Atotech Deutschland GmbH (Simon Bamberg, Frank Bruening, Ralf Bruening, Christoph Genzel, Laurence Gregoriades, Tanu Sharma)* | | | Thermal Cycle Consideration in Applying Lead-Free TFBGA Simulation to a Design *Yi-Chuan Tsai, National Sun Yat-Sen University* | | A friction based approach for modeling wire bonding *Simon Althoff, University of Paderborn (Walter Sextro, Tobias Hemsel, Jan Neuhaus)* |

# Tuesday Keynote

## October 1, 2013

### Opening Ceremonies: Annual Business Meeting, Awards Ceremony, Keynote

11:00 AM – 5:00 PM Exhibit Hall Opens
11:25 AM – 11:40 AM Annual Business Meeting
11:40 AM – 12:00 PM IMAPS Society Awards Ceremony

12:00 PM – 12:45 PM

### Junior Ballroom F

**KEYNOTE:**

### Next Generation of Electronic Systems - Challenges and Solutions for System Integration Technologies

The use of micro-level integration technologies to manufacture high-end electronic systems has increased dramatically around the world, the potential for applications being almost unlimited. To enable a smart planet, driven partly by the internet of things, next generation of electronic systems are expected to be more energy efficient, highly miniaturized and multifunctional with embedded computing, communication and sensing functionalities. In order to achieve this goal, novel heterogeneous system integration technologies and design methodologies are needed.

In this talk, some of the key system integration technologies required for the development of next generation electronic systems will be discussed. The focus will be on 3D wafer level packaging, panel level packaging and on interposer technologies. An overview of innovative electrical, thermal and thermo-mechanical design approaches will also be given.

**Prof. Dr. -Ing. Dr. sc. techn. Klaus-Dieter Lang - Klaus-Dieter Lang** is a Professor with the School of Electrical Engineering and Computer Sciences at the Technical University Berlin, Germany, where he leads research activities in the area of Nano Interconnect Technologies. He is also the Director of the Fraunhofer Institute for Reliability and Microintegration, IZM, Berlin.

Professor Lang began his career as a Research Engineer at Humboldt University Berlin, where he spent 10 years (1981 to 1991) working in the areas of Microelectronic Assembly, Packaging and Quality Assurance. In 1991, he moved to SLV Hannover to build up a Department for Microelectronic and Optic Components Manufacturing. He joined Fraunhofer IZM 20 years ago and was initially responsible for R&D activities in the area of Chip Interconnection Technologies. From 2001 to 2005 he coordinated Fraunhofer IZM's Lab on Microsystem Engineering in Berlin-Adlershof, and from 2003 to 2005 he was the Head of the Department of Photonic and Power System Assembly. In 2006, he was appointed as the Deputy Director of Fraunhofer IZM, a position he held till 2010. Since 2011 he has been the Director of the Institute.

Professor Lang Chairs the German Chapter of IEEE-CPMT and he is a member of numerous scientific boards and conference committees. He is the author and co-author of 3 books and more than 130 publications in the field of Wire Bonding Technologies, Microelectronic Packaging, Microsystems Technologies and Chip-on-Board Technologies. He studied Electrical Engineering at the Humboldt University Berlin, and holds a Master's degree and two Doctorate degrees.

12:45 PM – 2:00 PM Lunch Break (Food not provided by IMAPS Today)

'Orlando Aerial View

# Tuesday, October 1
# 1:30pm – 4:30pm in the Exhibit Hall
# Student/University Poster Session

Chairs: Venky Sundaram, Georgia Tech University; Tom Weller, University of South Florida; Ege Engin, San Diego State University; and Mike Newton, Newton Cyberfacturing

*One-on-One Interactive Forum. This is your chance for detailed interaction with student authors whose work is too good to miss.*

**Integrated Ψ-Type Photonic Polarization Diversity Receivers for Wireless Radio-over-Fiber Communication Links**

Vitaly Rymanov, Universitat Duisburg-Essen (Sebastian Dolme, Melanie Wachholz, Merih Palandaken, Tolga Tekin, and Andreas Stahr)

**Self-packaged High-Temperature Sensors for Harsh-Environment Applications**

Haitao Cheng, University of Central Florida (Xinhua Ren, Siamak Ebadi, Yaohan Chen, Linan An, Xun Gong)

**The Path Forward: Silicon Optical Modulator for CMOS ICs**

Kaikai Xu, University of California, Irvine

**Non-contact microwave characterization of printed resistors**

Maria F. Cordoba-Erazo, University of South Florida (Thomas M. Weller)

**Through Silicon Via (TSV) Arrays for High Frequency Signal Transmission in 3D Integrated Circuits**

Min Xu, CNSE, University at Albany (Robert Geer, University at Albany; Pavel Kabos, Thomas Wallis, NIST)

**Silver Oxalate: Towards a New Solder Material for Highly Dissipative Electronic Assemblies**

K. Kiryukhina, CNES (H. Le Trong, P. Tailhades, J. Lacaze, F. Courtade, S. Dareys, O. Vendier, L. Raynaud)

**Study of Wirebonding on Thin Al Pads with Various Size Probe Marks**

Shashi Sharma, Brigham Young University (Stevan Hunter, ON Semiconductor; Andrew Forhan, University of Colorado; Prakash Subedi, Dustin Whittaker, Brigham Young University)

**Design for Solder Joint Fatigue Life of BGA Package Subject to Mechanical Environment**

Jia-Shen Lan, National Sun Yat-sen University (Mei-Ling Wu)

**Excimer Laser Machining of Fired LTCC for Selectively Metalized Open Micro-channel Structures**

Dilshani Rathnayake-Arachchige, Loughborough University (Paul Conway, David Hutt)

**Compact Photonic Package for High-Power E-band (60-90 GHz) Photoreceiver Modules**

Vitaly Rymanov, University Duisburg-Essen (Merih Palandoken, Sebastian Duelme, Tolga Tekin, Andreas Stohr)

**Modeling and Reliability Analysis of TSVs for High Frequency Applications**

Kaushal Kannan, City College of New York (Sukeshwar Kannan, Bruce Kim)

**Droplet-on-Demand Inkjet-filled TSVs as a Pathway to Cost-efficient Chip Stacking**

Jacob Sadie, University of California, Berkeley (Niels Quack, Ming Wu, Vivek Subramanian)

**Thermal Cycle Consideration in Applying Lead-Free TFBGA Simulation to a Design**

Yi-Chuan Tsai, National Sun Yat-Sen University

**Effect of ENEPIG Surface Finish on the Vibration Reliability of Solder Interconnects**

Sandeep Menon, CALCE, University of Maryland (Adam Pearl, Michael Osterman, Michael Pecht)

**Thermal Cycling Reliability of Alternative Low-Silver Tin-based Solders**

Elviz George, CALCE, University of Maryland (Michael Osterman, Michael Pecht, Richard Coyle, Richard Parker, Elizabeth Benedetto)

**Conceptual Development Using 3D Printing Technologies for 8kV SiC Power Module Package**

Haotao Ke, North Carolina State University (Douglas Hopkins)

**A Switched-Line Microwave Phase Shifter Fabricated with Additive Manufacturing**

Jonathan O'Brien, University of South Florida (Mike Newton, Thomas Weller, Daniel Silva, Eduardo Rojas)

**Chip Design of an 1 V RF Receiver Front-End for 5.8-GHz DSRC Applications**

Wen Cheng Lai, National Taiwan University of Science and Technology (Jhin-Fang Huang, Yong-Jhen Jiangn)

**Fatigue Life Analysis of Sn96.5Ag3.0Cu0.5 Solder Thermal Interface Material of a Chip-Heat Sink Assembly in Microelectronic Applications**

Mathias Ekpu, University of Greenwich (Raj Bhatti, Michael Okereke, Kenny Otiaba)

**Thermo-Mechanical Stress of Underfilled 3D IC Packaging**

Ming-Han Wang, National Sun Yat-Sen University (Mei-Ling Wu)

**Stitch Bond Process of Pd-Coated Cu Wire: Experimental and Numerical Studies of Process Parameters and Materials**

Alireza Rezvani, University of Waterloo (Michael Mayer, Ivy Qin, Jon Brunner)

**Reliabilities and Strength of Al 718 For Thermoelectric Generator Assembly**

Victor Wolemiwa, University of Idaho (Dominic Nwoke)

**Modeling of Failure in Aluminum Alloy Braze for a High Temperature Thermoelectric Assembly**

Shams Arifeen, University of Idaho (Gabriel Potirniche, Aicha Elshabini, Fred Barlow)

# Tuesday, October 1, 2013 — Salon Rooms 1-6

| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| 2:00 PM –6:35 PM | **Advanced Platform Integration**<br>*Chairs: Urmi Ray, Qualcomm; Kyu-oh Lee, Intel*<br>This session addresses diverse platform integration schemes using 2.5 and 3D technologies. The papers address effective methodologies for design to electrical characterization with product applications as final target. Technology engineers and product managers will benefit from the breadth of technologies covered in the papers. | **Modeling and Design for SI and Reliability**<br>*Chairs: Chris Pan, Qualcomm; Judy Priest, Cisco*<br>Advanced modeling and simulation techniques are used to analyze and optimize electrical performance and reliability in silicon, substrates, packages, and L1/L2 assembly. Some measurement correlation may be discussed, along with printed circuit board effects. | **Polymers, Underfill, Encapsulants and Adhesives**<br>*Chairs: Jeff Gotro,Innocentrix; Lyndon Larson, Dow Corning*<br>In this session, we focus on some of the advances from the polymeric materials side; introducing novel adhesives, flux, and underfill technologies for use in a wide range of applications including molding, SMT, 2.5D and 3D assembly processes. | **Wirebonding & Stud Bumping**<br>*Chairs: Dan Evans, Palomar Technologies; Lee Levine, Process Solutions Consulting*<br>This session covers non-destructive testing challenges and methods of wires and bond pads, Pd-Coated Copper wire process window optimization, Copper wedge bonding, Al and Silver based wires as alternatives to copper, plus hybrid wire bond capabilities. | **Emerging Technologies**<br>*Chairs: Susan Bagen, Endicott Interconnect; Igor Prikhodko, Analog Devices*<br>In this session, novel structural materials will be introduced in conjunction with emerging applications. Specifically, applications in nanotechnology, MEMS sensors, counterfeit technologies, high-density data storages will be presented. Engineers will find this session helpful to explore alternative design choices for selecting technologies and materials for next generation products. | **Asian Perspective on Electronic Packaging and System Integration**<br>*Chairs: Tae-Kyu Lee, Cisco; Woongsun Lee, SK Hynix*<br>This special session covers the Asian perspective on electronic packaging. 3D, new material and process, and MCP, variety of packages are discussed in this session and distinguished speakers will present leading edge technologies of electronic packaging in Asia. |
| 2:00 PM –2:25 PM | Enabling a Manufacturable 3D Technologies and Ecosystem Using 28nm FPGA with Stack Silicon Interconnect Technology<br>*Woon-Seong, Kwon, Xilinx (Myongseob Kim, Jonathan Chang, Suresh Ramalingam, Liam Madden, Xilinx; Genie Tsai, Stephen Tseng, J.Y. Lai, Terren Lu, Steve Chiu, SPIL)* | Flip-Chip Packages with Periphery Cu Pillar Bumps as Wirebond Replacement - Design, Modeling & Characterization<br>*Zhe Li, Altera Corporation (Yee Huan Yew, Siow Chek Tan, Hui Lee Teng)* | A Novel High Thermal Conductive Underfill for Flip Chip Application<br>*Wusheng Yin, YINCAE Advanced Materials, LLC (Mary Liu)* | Non-Destructive Top Layer Bond Pad Cross Section<br>*Terence Collier, CVInc (Indira Gubeljic)* | DNA Marking: Implementation of a Proactive Counterfeit Risk Mitigation Solution<br>*Janice Meraglia, Applied DNA Sciences* | **FEATURED SPEAKER**<br>An Overview of Thin-Thin-Wafer Handling (with a Heat-Spreader Wafer) for 3D IC Integration<br>*John Lau, ITRI (Chun-Hsien Chien, Hsiang-Hung Chang, Wen-Li Tsai)* |
| 2:25 PM –2:50 PM | DIMM-in-a-Package (DIAP) Signal Integrity for High-Performance On-Board Memory Applications<br>*Zhuowen Sun, Invensas (Kevin Chen, Richard Crisp)* | Package Technology Selection of 28nm High Power FPGA with Pb-Free Bumps: Flip Chip Molded BGA Versus Traditional Bare Die Package<br>*Corey Reichman, Amkor Technology (Intel Corp - Michael Lyakas, Aaron Elberg, Romina Mimi Ocampo, Altaf Hasan, DierdreHale & Amkor - Miguel Jimarez, Fred Hamilton, Joon Dong Kim)* | An overview of molded underfill in flip chip packaging applications<br>*Fernando Roa, Amkor Technology* | Stitch Bond Process of Pd-Coated Cu Wire: Experimental and Numerical Studies of Process Parameters and Materials<br>*Alireza Rezvani, University of Waterloo (Michael Mayer, Ivy Qin, Jon Brunner)* | Transferable Redistribution Layers (TRDL)<br>*David Herndon, Harris Corporation (Suzanne Dunphy, Thomas Reed)* | Electroless Ni Plating Solutions for Reproducible Black Pad Analyses<br>*Jin Yu, Korea Advanced Institute of Science and Technology (KAIST) (K.H. Kim , Carnegie Mellon University)* |
| 2:50 PM –3:15 PM | High Speed Signal Transmission using Through-Si Vias and Coplanar Waveguides in a 3D IC Test Structure<br>*Min Xu, CNSE, University at Albany (Robert Geer, University at Albany; Pavel Kabos, Thomas Wallis, NIST)* | Modeling and Reliability Analysis of TSVs for High Frequency Applications<br>*Kaushal Kannan, City College of New York Sukeshwar Kannan, Bruce Kim)* | Packaging Materials for 2.5/3D Technology<br>*Brian Schmaltz, NAMICS Corporation* | Cu Heavy Wirebonding for High Power Device Interconnection<br>*Baik-Woo Lee, Samsung Advanced Institute of Technology (Chang-Sik Kim, Changmo Jeong, Younghun Byun, Jeong-Won Yoon, Che-Heung Kim, Seong Woon Booh, U-in Chung)* | Implementing Inductor Function with Vibrating Capacitor Structures<br>*Thomas Marinis, Draper Laboratory (Joseph Soucy)* | Scaling Challenges of Semiconductor Packaging in the Era of Big Data<br>*Yasumitsu Orii, IBM Research Tokyo* |

**DESSERT "HAPPY HOUR" & COFFEE BREAK IN EXHIBIT HALL: 3:15 PM - 4:30 PM**

**IMAPS Cafés sponsored by:**

**Dessert "Happy Hour" Sponsor:**

## Tuesday, October 1, 2013 — Salon Rooms 1-6

| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| 4:30 PM –4:55 PM | Electrical Characterization of TSVs with Varying Process Knobs and Temporary Bond/Adhesive System Robustness Studies for 2.5D/3D Manufacturing *Niranjan Kumar, Applied Materials (Sesh Ramaswami, Arvind Sundarrajan, CH Toh, Aksel Kitowski, Anthony C-T Chan, David Erickson, Jay Vijayen, Minrui Yu, Uday Mahajan)* | Design for Solder Joint Fatigue Life of BGA Package Subject to Mechanical Environment *Jia-Shen Lan, National Sun Yat-sen University (Mei-Ling Wu)* | Thermo-Mechanical Stress of Underfilled 3D IC Packaging *Ming-Han Wang, National Sun Yat-Sen University (Mei-Ling Wu)* | Multipurpose Wire Bonding - Bumps, Wires, Combination Interconnects, and Operation Efficiency *Daniel Evans, Palomar Technologies (David Rasmussen)* | Embedded Photonics Interconnect Eco-system for Data Center Applications *Richard Pitwon, Xyratex Technology Ltd (Alex Worrall, Kai Wang)* | High Thermal Conductive Inter Chip Fill for 3D-IC through Pre-applied Joining Process *Yasuhiro Kawase, Mitsubishi Chemical Corporation (Ikemoto, M. Sugiyama, M.Yamazaki, H. Kiritani, F. Mizutani, K. Matsumoto, A. Horibe, H.Mori, Y.Orii)* |
| 4:55 PM –5:20 PM | Polymer Based Interposer Providing ESD and Thermal Robustness *Karen Shrier, Electronic Polymers Newco Inc.* | Warpage Characterization and Improvements for IC Packages with Coreless Substrate *Bora Baloglu , Amkor Technology (Wei Lin, Danny Brady, Ken Stratton, Miguel Jimarez)* | Solder Joint Encapsulant Adhesive - LGA High Reliability And Low Cost Assembly Solution *Wusheng Yin, YINCAE Advanced Materials, LLC (Mary Liu)* | Automated Wirebond Pull Testing - Parallelogram of Forces-Real time Application *Richard C. Garcia, Crane Aerospace (Josef Sedlmair, F&K Delvotec)* | Decision Making Model for the Emerging Nanotechnologies *Kewal Verma, BCA International (Audre Dixon)* | Development of Organic Multi Chip Package for High Performance Application *Noriyoshi Shimizu, Shinko Electric Industries Co., LTD.* |
| 5:20 PM –5:45 PM | | | Adhesion and Cure Mechanism Studies for Advanced Lidded Flipchip Applications *Larson, Lyndon, Dow Corning Corporation (Kristen Steinbrecher, James Tonge)* | Thick Copper and Aluminium Wire Bonding Technology for High Power Laser Devices *Kong Weng Lee, JDS Uniphase (Jay Skidmore, Lei Xu)* | Ultra-Thin Zirconia Ceramic Membranes for Electronic Applications *John Olenick, ENrG, Inc.* | Thermally Activated Bumping Process of Sn3.0Ag0.5Cu Solder for Low-Cost Interposer *Kwang-Seong Choi, ETRI (Haksun Lee, Hyun-Cheol Bae, Yong-Sung Eom)* |
| 5:45 PM –6:10 PM | | | | Study of Wirebonding on Thin Al Pads with Various Size Probe Marks *Shashi Sharma, Brigham Young University (Stevan Hunter, ON Semiconductor; Andrew Forhan, University of Colorado; Prakash Subedi, Dustin Whittaker, Brigham Young University)* | A Study on Prevalent Factors Behind Efficiency Deterioration of a Typical Low Power Solar Panel *Virgil Ganescu, Education Affiliates* | Low Temperature Si-Si, SiO2-SiO2 Covalent Bonding with Thin Siloxane Layer *Jeong-Yub Lee, Samsung Advanced Institute of Technology* |
| 6:10 PM –6:35 PM | | | | High Speed Aluminum Wirebonding for Molded Packages *Luu Nguyen, Texas Instruments Inc. ( Ken Pham, Anindya Poddar, Texas Instruments; Yoshihito Hagiwara, Naoki Sekine, Shinkawa)* | | |

## Wednesday, October 2, 2013 — Salon Rooms 1-6

| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| 8:00 AM –11:15 AM | **Packaging Transitions: 2.5D and 3D Interconnect Technologies from Wire Bond to RDL to TSV**<br>*Chairs: Greg Caswell, DfR Solutions; Cristina Chu, TEL NEXX*<br>The transition from packaging today as we know it to true 3D interconnects involves many hybrid solutions as the industry inches towards TSVs. This session will focus on creative implementations of packaging to efficiently push the boundaries of RDLs, bumping and interposers, among other applications, to cost effectively address the challenges delivering the greatest electronic efficiency at the lowest prices. | **Thermal and Thermo-Mechanical Modeling**<br>*Chairs: David Saums, DS&A LLC; Mary Cristina Ruales Ortega, University System Ana G. Mendez*<br>This session focuses on thermal and thermo-mechanical modeling. A variety of topics will highlight recent advances within these areas. | **Substrate Materials I**<br>*Chairs: Michael Folk, Northrop Grumman Corp.; Jeff Hartman, Northrop Grumman Corp.*<br>Improved substrates and associated processes are required to improve performance, reliability and lower cost of ownership. In this session the properties and processes for advancing substrates will be presented. | **Flip Chip Bumping**<br>*Chairs: Andy Strandjord, Pac Tech USA; Nick Renaud-Bezot, AT&S*<br>Solder bumping is a reliable interconnect technology that is directly compatible with many of the latest semiconductor technologies, including: 2D, 3D, organic packages, and ultra thin packages. Continued reliability testing, process development, and materials development are essential to ensure that solder bumping is a long-term interconnect solution as these new semiconductor technologies evolve. | **New Concepts, Interconnects & Processes for High Performance Packaging**<br>*Chairs: Benson Chan, Endicott Interconnect; Ron Lasky, Indium Corporation*<br>In this session, novel concepts, interconnects and processes for next high performance packaging will be presented. | **Power Packaging I**<br>*Chairs: Mark Hoffmeyer, IBM Corporation; Doug Hopkins, North Carolina State University*<br>This session focuses predominantly on power packaging systems, electrical design, modeling, and the deployment of advanced power packaging applications. |
| 8:00 AM –8:25 AM | Cost Comparison of 2.5D/3D Packaging to other Packaging Technologies<br>*Chet Palesko, SavanSys Solutions LLC (E. Jan Vardaman, TechSearch International, Inc.; Alan Palesko, SavanSys Solutions LLC)* | Interactions between Variable Frequency Microwave Underfill Processing and High Performance Packaging Materials<br>*Mamadou Diobet Diop, Universite de Sherbrooke (Dominique Drouin, Universite de Sherbrookek; Marie-Claude Paquet, IBM Canada)* | Effects of Copper Pattern Density and Orientation on the Modulus of BGA Substrates<br>*Burton Carpenter, Freescale Semiconductor, Inc (Betty Yeung, Freescale Semiconductor, Inc; Yuan Yuan)* | Development of an Ultra Thin Die-to-Wafer Flip Chip Stacking Process for 2.5D Integration<br>*Gabriel Pares, CEA-Leti (A. Attard, F. Dosseul, G. Klug, G. Simon)* | Si Vapor Chamber Integrated with Through Silicon Via for 3D Packaging<br>*Jun Taniguchi, Fujitsu Laboratories LTD. (Takeshi Shioga,Yoshihiro Mizuno)* | Energy Efficient Electronics: An objective, a resource, a market<br>*Jeff Perkins, Energy & Resource Solutions* |
| 8:25 AM –8:50 AM | Redistribution Layers (RDLs) for 3D IC Integration<br>*John Lau, ITRI (Pei-Jer Tzeng, Ching-Kuan Lee)* | Heatsink Induced Thermo-mechanical Strain in QFN Devices<br>*Gerard McVicker, IBM Research (Vijay Khanna, Sri M. Sri-Jayantha)* | A photo-desmear method for via residue removal using a VUV light source<br>*Tomoyuki Habu, Ushio Inc. (Shintaro Yabu, Kenichi Hirose, Hiroki Horibe, Ushio, Inc.; Toru Fujinami, Ushio America; Naoki Kitano, Eiji Ozawa, Intel K.K.; Sanchali Bhattacharjee, Ebrahim Andideh, Daniel Sobieski, Intel Corp.)* | Long-term Electromigration Study of Lead-Free Flip-Chips with Solder Bumps with 50 $\mu$m or 60 $\mu$m Diameter Employing ENIG Surface Finish on Both Chip and Substrate Side<br>*Marek Gorywoda, University of Applied Sciences Hof (Rainer Dohle, Andreas Wirth, Jörg Goßler, Micro Systems Engineering GmbH; Stefan Härter, Jörg Franke, University of Erlangen-Nuremberg)* | Inspection and Metrology Solutions for Cu Pillar and TSV High-Volume Manufacturing<br>*Rajiv Roy, Rudolph Technologies (Matt Wilson, Darren James)* | The Next Level of Accurate Server Power Monitoring and Capping<br>*Jerry Steele, Texas Instruments* |

# Wednesday, October 2, 2013 — Salon Rooms 1-6

| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| **8:50 AM –9:15 AM** | A Wide I/O Memory-on-Logic Product Prototype Enabled by Through Silicon Stacking Technology *V. Ramachandran, Qualcomm Technologies, Inc. (D. W. Kim, S. Gu, R. Lindley, B. Henderson, U. Ray, R. Radojcic, M. Nowak, A. Gunterus, A. Cassier, Qualcomm Technologies, Inc.; Sharon Chen, M.F. Chen, C.H. Wu, S.P.Jeng, C.H. Yu, Taiwan Semiconductor Manufacturing Company, Ltd.)* | Fatigue Life Analysis of Sn96.5Ag3.0Cu0.5 Solder Thermal Interface Material of a Chip-Heat Sink Assembly in Microelectronic Applications *Mathias Ekpu, University of Greenwich (Raj Bhatti, Michael Okereke, Kenny Otiaba)* | Method to Measure the Effects on Surface Roughness on the High Frequency Transmission Line *Toshiki Iwai, Fujitsu Laboratories Ltd. (Daisuke Mizutani, Motoaki Tani)* | 3D Integration of System-in-Package (SiP) Using Organic Interposers: Toward SiP-Interposer-SiP for High-End Electronics *Rabindra Das, Endicott Interconnect Technologies, Inc. (Frank Egitto, Steven Rosser, Erich Kopp, Barry Bonitz)* | Multi Beam Low-K Grooving Evaluation of Various Removal Principals-ALSI *Jeroen van Borkulo, Advanced Laser Separation International (ALSI) N.V. (Henry de Jonge)* | Package design and development of a low cost high temperature (250°C), high current (50+A), low inductance discrete power package for advanced Silicon Carbide (SiC) and Gallium Nitride (GaN) devices *Brice McPherson, APEI, Inc. (Brandon Passmore, Peter Killeen, Daniel Martin, Ty McNutt)* |
| | **COFFEE BREAK IN EXHIBIT HALL: 9:15 AM – 10:00 AM — sponsored by LORD AskUsHow™ (Exhibit Hall Open: 9:00 AM – 7:30 PM)** | | | | | |
| **10:00 AM –10:25 AM** | 3D RCP Package Stacking: Side Connect, An Emerging Technology for System Integration and Volumetric Efficiency *Michael Vincent, Freescale Semiconductor, Inc. (Doug Mitchell, Jason Wright, Alan Magnus, WengFoong Yap, Jinbang Tang, Scott Hayes)* | Thermally and Electrically Enhanced Wirebond BGA *Burton Carpenter, Freescale Semiconductor, Inc (Boon Yew Low, Leo Higgins III, Sriram Neelakantan, Robert Wenzel, Daniel Boyne)* | Analysis of the Thick Film Deposited on Alumina Substrate and Effect of Different Parameters on the Response of Propanol Using Taguchi Method *Ibrahim Gaidan, Sirite University* | Organic Chip Scale Package (CSP) Development for Flip Chip Applications *Tomoyuki Yamada, Kyocera SLC Technologies (Masahiro Fukui, Kenji Terada, Masaaki Harazono, Teruya Fijisaki, Kyocera SLC Technologies ; Tomoyuki Yamada, Kyocera; Jean Audet, Sushumna Iruvanti, Yi Pan, Scott Moore, Brian Sundlof, Charlie Reynolds, IBM Corporation)* | Stencil Printing Process Guidelines for 0.3mm Pitch Chip Scale Packages *Mark Whitmore, DEK Printing Machines Ltd (Jeff Schake, Clive Ashmore)* | Advanced Thermal Simulation Model for Power MOSFETs *Jens Ejury, Infineon Technologies N.A. Corp* |
| **10:25 AM –10:50 AM** | 3D Integrated Packaging Approach for High Performance Processor-Memory Module *Stephen Polzer, Mayo Clinic (W. L. Wilkins, J. L. Fasig, M. J. Degerstrom, B. K. Gilbert, E. S. Daniel)* | Accurate Finite Element Analysis of Embedded Wafer Level Packaging by Thermomechanical Characterization of Materials and ICs Piezoresistive Stress Sensors *Sinh Vuhoang, Ecole Nationale Superieure des Mines de Saint-Etienne (ENSM-SE) (J.Mazuir, M.Bella, C.Bouvier, G.ParÃ¨s, K.Martinschitz, H.Wiesbauer, C.Rivero, A. Planchais, M. Saadaoui)* | RF Capacitor Material for Use in PCBs *Jin-Hyun Hwang, Oak-Mitsui Technologies, LLC (John Andresakis, Ethan Feinberg, Bob Carter, Yuji Kageyama, Fujio Kuwako)* | Improving WLCSP Reliability Through Solder Joint Geometry Optimization *Boyd Rogers, Deca Technologies (Chris Scanlan)* | Z-Axis Interconnection: A Versatile Technology Solution for High Performance Electronics *Rabindra Das, Endicott Interconnect Technologies, Inc. (J. M. Lauffer, F.D. Egitto)* | A Highly Integrated GaAs-based Module for DC-DC Regulators *Greg J. Miller, Sarda Technologies (Bogdan Duduman, Bill Batchelor)* |
| **10:50 AM –11:15 AM** | Next-Generation Lead-Free Solder Plating Products for High Speed Bumping, Capping and Micro-Capping Applications *Jonathan Prange, The Dow Chemical Company (Julia Woertink, Yi Qin, Pedro Lopez Montesinos, Inho Lee, Yil-Hak Lee, Masaaki Imanari, Jianwei Dong, Jeff Calvert)* | Evaluation of Thermal Performance for a New Ventilated Heat Sink Module *Shiang-Jiun Lin, National Kaohsiung University of Applied Sciences (Yen-Wei Chen)* | Characterization of CVD Diamond for Thermal Management Applications *Brooke Locklin, Element Six (Richard Balmer, Thomas Obeloer)* | Isothermal Fatigue Tests of Sn63-Pb37,Sn62-Pb36-Ag2 and Sn42-Bi58 Solder Joints *Eliane M Grigoletto, UNISAL College (Itamar Ferreira)* | | |

# Wednesday Keynote

## October 2, 2013

9:00 AM – 7:30 PM Exhibit Hall Opens
12:15 AM – 1:30 PM Lunch in Exhibit Hall (Lunch Provided by IMAPS & Sponsors)

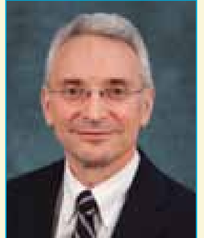
11:20 AM – 12:05 PM

### Junior Ballroom F

**KEYNOTE:**

### Progress in Developing an Open Supply Chain for 2.5D/3D Market Enablement

An open supply chain requires close collaboration, early investment, and focus on the ultimate goal of yield and cost to enable markets. An open supply chain is more complex to develop but will provide the end-customer with the most flexibility and transparency and enables use of expertise in each stage of the supply chain. An open supply chain also requires high levels of sharing, not typical in our industry. Significant progress has been made in test chip development, TSVs, interposers, test strategy, yield, and cost. Data and remaining challenges will be presented in each of these areas. The relationship between memory architecture and cost will also be discussed.



**David McCann** is Vice President of Packaging at GLOBALFOUNDRIES in Malta, New York. In this role, David is responsible for Packaging R+D, interconnect development, and back-end strategy and implementation. David started at GLOBALFOUNDRIES in 2011.

Prior to GLOBALFOUNDRIES, David worked at Amkor Technology for 11 years, in product group and development roles. He also led cross-functional teams including networking product strategy and mobile product development.

David has supported the Electronic Component and Technology Conference for more than 10 years. He was General Chair in 2012.

David McCann received his Masters in Engineering Management from the Santa Clara University in 1985 and his BS in Ceramic Engineering from the University of Illinois in 1981.

Downtown Orlando around Lake Eola

# GLOBAL BUSINESS COUNCIL (GBC)
## Keynote Luncheon & Market Forecasting Analyst Session
## Wednesday, October 2, 2013 — in the Junior Ballroom

Global Business Council

*Keynote Lunch Sponsored by:*

**Complimentary for all to attend, thanks to our Sponsor: Sikama**

*Limited Seating - 75 Seats Available • (first come first served - visit the registration desk to reserve your seat)*

### Junior Ballroom G

12:30 PM: Welcome Message: **GBC Objectives and Agenda Review**

*Lee Smith, Plexus Corp.*

12:40 - 1:00 PM: GBC Luncheon & Keynote Speaker: **"The Microelectronics Industry in Brazil"**

*Claudius Feger, IBM Research - Brazil, feger@us.ibm.com*

As Brazil's middle class has increased by 35 million people, electronics imports have skyrocketed - resulting in a narrowing of Brazil's trade balance, which in January 2013 turned negative. To address this trend, the Brazilian government made the development of a local microelectronics industry an economic priority. Previously, the government focused on developing IC design skills and the creation of design houses, of which 22 were established to-date. However, the success of these has been limited, mostly because of difficulties in attracting industrial projects and thus over half of the existing design houses are not for profit.

With the announcement in late in 2012 of the creation of SIX Semicondutores, an IDM which once completed, will be the most advanced, commercial chip manufacturer in Latin America, the Brazilian microelectronics industry started a new chapter. SIX Semi will be using IBM 130 and 90 nm technology to provide advanced mixed signal / hybrid semiconductor devices and products for the medical devices, smart card, sensor, energy management and similar markets. In doing so, Brazil hopes to start making a dent in the import of about US$4 - 5 billion annual imports of ICs.

Another focus area is electronic packaging. But even after the announcement in 2012 of HT Micron, (a joint venture between the Brazilian Altus and the Korean Hana Micron), this area will remain poorly served in Brazil, because HT Micron will focus exclusively on the highly competitive memory packaging segment.

Over the years the Brazilian government has instituted several laws and regulations to support the formation of an electronics industry with Brazilian content. This spans efforts from creating academic programs and research institutions to laws requiring industrial research investments to direct investments by the Brazilian development bank in industries. However many hurdles remain.

This talk will describe successes and hurdles in the development of a successful microelectronics ecosystem in Brazil and will provide an up-to-date picture of this important emerging market.

1:00 - 2:00 PM: Industry Analyst & Panel Discussion

**"Addressing Major Changes in the Supply and Demand for Advanced Packaging Technologies"**

1:00 – 1:20 PM:

**"Demand Outlook for 2.5 / 3D and Wafer Level Packaging"**

*Yole Developpment – Christophe Fitamant, Sales & Marketing Director*

Wafer level packaging market is started to gain more and more significance in the semiconductor industry, showing a great potential for future growth. By 2017, the total number of wafers which will be manufactured using packaging technologies (bumping, TSV, RDL, etc.) is expected to reach 23% of the total IC semiconductor industry.

If historically, the wafer level packaging was mostly supported by flip-chip wafer bumping using electroplated gold and solder bumps, today the industry is benefiting from a large variety of different packaging technologies and platforms: WL Optics, 3D WLP, WLCSP (fan-in), Fan-out WLP, Embedded Dies, 2.5D and 3DIC and Flip Chip.

It is a real opportunity for the entire supply chain to work together and further consolidate and strengthen the system value-chain in order to fully take advantage of the benefits and advantages these packaging technologies bring.

In this talk, Yole Développement will look at the current status of the 3D Packaging industry, provide technical trends for 2.5 & 3D, Fan-In and Fan Out, Embedded Chip in Substrate packaging technologies as well as discuss further trends and forecasts projections for the next 5 years, highlighting the driving applications and their expected evolution.

1:20 – 1:40 PM:

**"Supply Chain Implications for Advanced Packaging"**

*Gartner Dataquest – Mark Stromberg, Senior Analyst*

Advanced packaging markets have been the major driver for back-end processing in recent years. Several device makers have stated that between the 30 and 20nm nodes essentially all their products will move to flip-chip and wafer-level type processes. This has, and will continue to, introduce new materials, production processes and equipment into the packaging space.

While advanced packaging has been a major growth segment, there are some competitive processes, particularly for the 3D Through Silicon Via (TSV) market that have shown some promise. TSV has been discussed as a major industry initiative for more than 5 years, but has yet to launch into mainstream markets and has been limited to very high end final electronic products such a file servers. Reasons for this include production costs and device yield concerns.

This discussion will be focused on the forecasts for bumping processes and 3D technologies. Technical, yield and cost issues for these advanced processes will also be presented. Gartner's most recent forecast for WLP equipment markets will be included in this presentation. Forecasts for the general packaging and test, WLP and TSV markets are also going to be reviewed during this talk.

1:40 – 2:00 PM:

**Panel Format with Audience Questions & Answers**

*Moderator – Lee Smith*

## Wednesday, October 2, 2013 — Salon Rooms 1-6

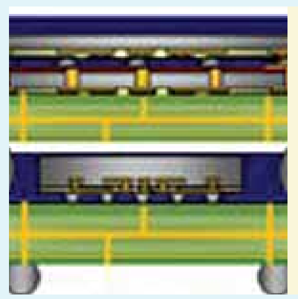
| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| **2:00 PM –5:30 PM** | **Glass Interposers**<br>*Chairs: Steve Annas, Triton Micro Tech; Aric Shorey, Corning Inc.*<br>As we rapidly increase requirements on packaging & interconnect performance, we approach the limits of today's technology, thus the need increases for a greater number of components in smaller packages using Silicon and Glass (TGV) emerging as the need for 2.5D & 3D passive Interposers grow to better support this next generation assembly. | **Testing Methods and Process for Improved Reliability**<br>*Chairs: Mike Ferrara, RF Micro Devices; Akhlaq Rahman, Thin Film Corp.*<br>In this session, novel characterization methods will be introduced as well as unique approaches to new material sets providing improved reliability. | **Substrate Materials II (Ceramic & LTCC)**<br>*Chairs: Dan Krueger, Honeywell FM&T; Ken Peterson, Sandia National Labs.*<br>New and evolving applications, designs, and characterization of ceramic and low temperature cofired ceramic (LTCC) packaging solutions are provided in this session. Radio Frequency (RF), microfluidics, high power applications are all explored in this diverse session exploring the versatility of ceramic and LTCC substrate systems. | **MEMS & Sensor Packaging**<br>*Chairs: Matt Apanius, SMART Commercialization Center for Microsystems; Ron Jensen, Honeywell*<br>Packaging plays a critical role in the robustness associated with MEMS and sensor performance. As the applications tend to be quite varied, the interfaces between the sensor, package, electronics, and media need to be well-defined. Unique solutions for MEMS and sensor packaging interfaces will be presented in this session. | **Think Thin: Thin IC Packaging For Mobile Devices**<br>*Chairs: Rich Rice, ASE; Jason Cho, ASE; Milind Shah, Qualcomm*<br>The objective of the "Think Thin" session is to address the numerous aspects of making IC packages "thinner". This session enables discussion and presentations on the latest materials, process, design, and emerging applications of "thin" packaging technology. | **Power Packaging II**<br>*Chairs: Julie Adams, UBOTIC Company Ltd.; Mark Hoffmeyer, IBM Corporation*<br>This session includes an array of topics spanning new materials, process advances reliability, circuit design, and application user considerations for optimized, state of the art power packaging applications. |
| **2:00 PM –2:25 PM** | Thermal Characteristic and Performance of the Glass Interposer with TGV (Through-Glass Via)<br>*Heng-Chieh Chien, Industrial Technology Research Institute (Chun-Hsien Chien, Ming-Ji Dai, Ra-Min Tain, Wei-Chung Lo, Yung-Jean Rachel Lu)* | Advanced Warpage Characterization for FOWLP<br>*Isabel Barros, Nanium, SA (Mario Ribeiro)* | Plating Reliability and High Frequency Testing of DuPont™ GreenTape™ 9K7 LTCC<br>*Allan Beikmohamadi, DuPont (Mike Champ, Patricia Graddy, Beth Hughes, Deepukumar Nair, Jim Parisi, Mike Smith, Steve Stewart)* | A Current-Controlled PCB Integrated MEMS Tilt Mirror<br>*Robert Dean, Auburn University (Colin Stevens, John Tatarchuk)* | Active and Passive Component Embedding Into Low-cost Plastic Substrates Aimed at Smart System Applications<br>*Maarten Cauwe, IMEC-Cmst (Bjorn Vandecasteele, Johan De Baets, Jeroen van den Brand, Roel Kusters, Ashok Sridhar)* | Electromigration in Pb-Free Solder: A Power IC Perspective<br>*Tom Wassick, IBM Systems and Technology Group* |
| **2:25 PM –2:50 PM** | Performance and Process Comparison between Glass and Si Interposer for 3D-IC Integration<br>*Chun-Hsien Chien, Industrial Technology Research Institute (Ching-Kuan Lee, Chang-Chih Liu, Hsun Yu, Peng-Shu Chen, Heng-Chieh Chien, Ming-Ji Dai, Yu-Min Lin, Shin-Yi Huang, Chia-Wen Fan, Jon-Shiou Peng, Chau-Jie Zhan, Cheng-Ta Ko, Shih-Hsien Wu, Ra-Min Tain, Wei-Chung Lo, Yung Jean Rachel Lu)* | An Analysis of Evolving Package Reliability Test Methodologies for Wireless Applications<br>*Michael Ferrara, RFMD* | Low Loss Power Distribution Network Design in Low Temperature Co-Fired Ceramic Technology<br>*Michael D. Glover, University of Arkansas (Michael C. Hamilton, Emmanuel Decrossas, Kaoru Maner, Alexander Pfeiffenberger, H. Alan Mantooth)* | High and Moderate-Level Vacuum Packaging of Vibratory MEMS<br>*Igor Prikhodko, University of California, Irvine (Brenton Simon, Gunjana Sharma, Sergei Zotov, Alexander Trusov, Andrei Shkel)* | Modular Microsystems with Embedded Components<br>*Christian Boehme, Fraunhofer IZM / TUB (Andreas Ostmann, Martin Schneider-Ramelow)* | Conceptual Development Using 3D Printing Technologies for 8kV SiC Power Module Package<br>*Haotao Ke, North Carolina State University (Douglas Hopkins)* |
| **2:50 PM –3:15 PM** | Glass Interposer Substrates: Fabrication, Characterization and Modeling<br>*Aric Shorey, Corning Incorporated (John Keech, Garrett Piech, Scott Pollard, Satish Chaparala)* | The Effectiveness of Screening Techniques for Revealing Cracks in High Volumetric Efficiency MLCCs<br>*Alexander Teverovsky, Dell Services Federal Government, Inc.* | Thick Film Pastes for Nitride Ceramics for High Power Applications<br>*Marco Wenzel, Fraunhofer IKTS (Richard Schmidt, Uwe Partsch, Markus Eberstein)* | Microfluidic Device Packaging<br>*Leland Spangler, Aspen Microsystems* | Size Matters - Embedding as an Enabler of Next-Generation SiPs<br>*Nick Renaud-Bezot, AT&S (Mark Beesley, Christian Galler)* | Improving System Performance with eGaN® FETs in DC-DC Applications<br>*David Reusch, Efficient Power Conversion (EPC) (Alex Lidow, Johan Strydom)* |

**COFFEE BREAK IN EXHIBIT HALL: 3:15 PM – 4:00 PM — sponsored by**

## Wednesday, October 2, 2013 — Salon Rooms 1-6

| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| 4:00 PM –4:25 PM | Development of TGV Interposer for 3D IC *Shintaro Takahashi, Asahi Glass Co., Ltd. (Kohei Horiuchi, Kentaro Tatsukoshi, Motoshi Ono, Masaki Mikayama, Nobuhiko Imajo, Vern Stygar, Tim Mobley)* | Dicing Development for Low-K Copper Wafers using Nickel-Palladium-Gold Bond Pads for Automotive Application *Tu Anh Tran, Freescale Semiconductor, Inc. (Wen Shi Koh, K. Y. Yow, Y. K. Au)* | Low Temperature Co-fired Ceramic (LTCC) Technology for Development of Components/Devices for Alternative Applications *Hansu Birol, Centro de Inovacoes CSEM Brasil (Sergio Lopera, Warner Bernardes Quintao, Erika Gyoervary, James Buntaine, Tiago Alves)* | Void Formation and Bond Strength Investigated for Wafer-level Cu-Sn SLID Bonding *Astrid-Sofie B. Vardoy, SINTEF ICT (H.J. van de Wiel, Stian Martinsen, Marcel Kouters, Greg Hayes, Hartmut Fischer, Knut Aasmundtveit, Adriana Lapadatu, Maaike Taklo)* | Novel back-side grinding and laser dicing process for Cu pillar generated low-k wafer *Yuka Tamadate, Shinko (Hideki Maruyama, Katsunori Aoki, Takashi Ozawa, Haruo Sorimachi)* | Source-sense packages for HV MOSFETs *Anders Lind, Infineon Technologies North America Corp.* |
| 4:25 PM –4:50 PM | Challenges of Adhesion Promotion for the Metallization of Glass Interposers *Robin Taylor, Atotech Deutschland GmbH (Simon Bamberg, Michael Merschy, Tobias Bernhard, Frank Bruening)* | Immersion Tin for QFN-Packages to Create a 3-D Solder Joint for Reliability Enhancement *Mustafa Oezkoek, Atotech (Hubertus Mertens, Jerome Bender, Atotech Deutschland GmbH)* | | Mechanical Stress Analyses of Packaged Pressure Sensors for Very High Temperatures *Roderich Zeiser, University of Freiburg - IMTEK (Suleman Ayub, Juergen Wilde)* | High Bandwidth PoP *Jason Cho, ASE (US), Inc. (Mike Hung, Morris Cheng, Timmy Lin, Calvin Lee)* | Integrated Current Sensing Technology for Synchronous Buck Converters *Evan Reutzel, Texas Instruments Inc. (Scott Ragona, Rengang Chen, David Jauregui)* |
| 4:50 PM –5:15 PM | | A fully automated execution of complex DOE to characterize electroplating baths *Robert Forman, ancosys, Inc. (Norbert Schroeder)* | | Packaging CMUTs for Gesture Sensing *Luu Nguyen, Texas Instruments Inc. (Ira Wygant, Peter Johnson)* | Thin PoP For Mobile Devices - Conquering Technological and Process Challenges To Meet Customer Demands *Sachin Deo, Micron Technology* | Detailed Analysis of How Power Stage and Power Clip Products Achieve Optimized Power Density *Arthur Black, Fairchild Semiconductor* |
| 5:15 PM –5:40 PM | | Improvement of Back-Side Cosmetic Defects And Wafer Strength *Erwin Cohen, IBM SRDC (Victoria L. Calero-DdelC, Irene Popova, Richard Indyk, Joe Sullivan, John Fitzsimmons; Aaron Bicknell, Lam Research)* | | | Compression Molding Solutions for Various High-end Package and Cost Savings for Standard Package Applications *CH Ang, Towa USA (Muneo Miura, Towa Corporation)* | |
| 5:40 PM –6:05 PM | | | | | Reducing Package Thickness to Accommodate Next Generation Smartphone Designs *Brian Roggeman, Qualcomm Technologies, Inc (Rajneesh Kumar, Mark Schwarz)* | |

**EXHIBIT HALL RECEPTION: 5:30 PM – 7:30 PM — sponsored by** APPLIED MATERIALS® micross components transforming specialty electronics



# Save the Date!
## Device Packaging 2014
### March 10-14, 2014 Fountain Hills, AZ

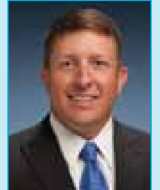
# Thursday, October 3, 2013 — Junior Ballroom F

**INTERPOSERS & 2.5/3D PACKAGING**

**8:00 AM –12:00 PM An entire morning of the conference dedicated to 2.5D & 3D IC, Interposers, Packaging…**

## 3D KEYNOTE PRESENTATIONS:

**8:00 AM – 8:45 AM**
**Micron's Hybrid Memory Cube – the New Standard for Memory Performance**



Yole Développement research analysts project a $40B market for TSV-enabled 3D devices by 2017— nearly 10% of the global chip business. These projections rely heavily on leading technologies such as the Hybrid Memory Cube (HMC) which represents a fundamental change in memory construction and connectivity.

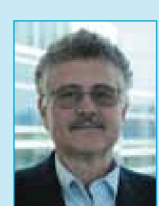
HMC is a three-dimensional structure with a logic device at its base and a plurality of DRAMs vertically stacked above it using through-silicon via (TSV) connections. In this talk, the HMC concept is analyzed, exploring how the DRAM functions are re-architected to deliver a scalable, energy efficient system architecture, delivering extremely high performance and resiliency. The presentation will also address how innovative and disruptive solutions such as HMC require equally innovative tools, ecosystems and go-to-market strategies.

***Scott Graham - General Manager, Hybrid Memory Cube Technology***
***Micron Technology, Inc.***

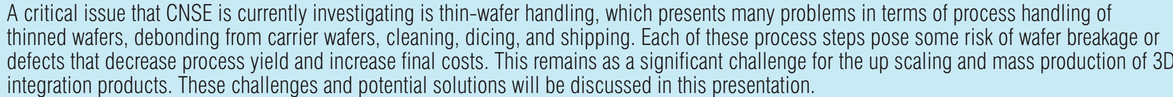
*Mr. Graham joined Micron in 1994 as an applications engineer in the personal computing division. He has held various managerial positions within Micron and has spent the last 11 years in Micron's memory products division, working on technical marketing for DRAM and NAND memory products. In recent years, Mr. Graham has represented Micron in various organizations responsible for setting industry standards, holding numerous vice-chair, chair, and board-level positions.*

*Mr. Graham holds a Bachelor of Science in Electronic Engineering Technology from DeVry University and a micro-MBA certification from Boise State University.*

**8:45 AM – 9:30 AM**
**Overview of Critical 3D Integration Challenges to Bring Products to Market**



The widespread adoption of 3D Integration is inevitable with many companies introducing products into manufacturing or beginning the latter stages of development [1-3]. In this talk, we will discuss three focus areas that need improvement and cost reduction in order to bring 3D integration into the mainstream.



A critical issue that CNSE is currently investigating is thin-wafer handling, which presents many problems in terms of process handling of thinned wafers, debonding from carrier wafers, cleaning, dicing, and shipping. Each of these process steps pose some risk of wafer breakage or defects that decrease process yield and increase final costs. This remains as a significant challenge for the up scaling and mass production of 3D integration products. These challenges and potential solutions will be discussed in this presentation.

The other area that is of high interest to the 3D community is the bonding method used to connect each layer of a 3D stack. Three types of bonding methods are examined: copper-to-copper (Cu-Cu) direct thermo-compression (TC) bonding, transient liquid phase bonding (Cu - Sn on Cu), and solder bonding. The benefits, cost, and technical obstacles of these techniques will be discussed.

Finally, important challenges for Assembly and Test ( with respect to OSATs) will be discussed. There is a significant gap between semiconductor manufacturing and OSATs with regards to 3D integration. Large Fabs have solved this issue in-house with fully integrated semiconductor and packaging solutions. However, the roadmap for the rest of the industry is unclear for packaging of 3D integrated die. This item will be discussed in terms of the expanding role of OSATs that will be required in order to successfully bring 3D integration products into the marketplace.

***Douglas Coolbaugh - Derivatives and 3DI Manager***
***College of Nanoscale Science and Engineering (CNSE) at Albany SUNY Nanofab***

*Douglas Coolbaugh received his PhD in Physical Chemistry from SUNY Binghamton, NY in 1987. Doug retired from IBM in 2010 after working 30 years in microelectronics development. Presently he is the Assistant VP of derivatives at the College of Nanoscale Science and Engineering.*

**9:30 AM – 10:15 AM**
**Contributing to 3D Interconnect (3DIC): One Toolmakers Approach to Meeting the Challenge**

For the last five of six years, identifying the requirements and metrics to meet 3D Interconnect high volume manufacturing (HVM) readiness has been a moving target. Will 3DIC happen in the front end of the line, advanced packaging or somewhere in between? From a toolmakers perspective, it is easy to get confused. It is a management challenge to fund programs one year that are redefined the following year. Finding solutions that will facilitate the transition to 3DIC is our professional obligation as responsible equipment manufacturers and corporate citizens.

At TEL NEXX, we see cost effective solutions as the most significant challenge to 3DIC implementation. During this talk, I will share two of the approaches we used at TEL NEXX to identify and test proposed 3DIC solutions. The first method has been to collaborate with our suppliers transparently in order to speed up development lifecycles and minimize scale up costs. The second method has been to explore alternative solutions outside of the traditional unit process flows in search of disruptive technologies. These strategies helped us offer our customers a path to progress towards 3DIC HVM readiness.

***Tom Walsh - President***
***TEL NEXX at Tokyo Electron***

*Dr. Tom Walsh is President of TEL NEXX at Tokyo Electron, a leading worldwide semiconductor equipment provider focused on building advanced packaging tools. Walsh led teams of semiconductor professionals to successfully deliver game changing technologies to the market, including the growth and eventual sale of NEXX Systems to Tokyo Electron for Advanced Packaging Deposition (2012), the development of the Novellus Sabre Plating system for Copper Interconnect (1998) and the commercialization of the IBM Atomic Force Microscope (1993). Over the past 25 years, Walsh held roles from scientist to corporate executive at IBM, Novellus and NEXX Systems. He holds a Ph.D. in analytical chemistry from Purdue University and an MBA from the Stern Business School at NYU.*

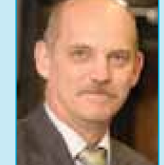
**10:15 AM – 10:30 AM: Coffee Break In Foyer — sponsored by**

**10:30 AM – 12:00 PM**
**3D IC PANEL DISCUSSION:**

**What are preventing 3D IC integrations from High Volume Manufacturing?**

***Moderator: John H. Lau, ITRI, Taiwan***

3D IC integration with through-silicon via (TSV) technology provides the opportunity for the shortest chip-to-chip and the smallest pad size and pitch interconnects. Compared with other interconnection technologies, the advantages of 3D IC integration include better electrical performance, lower power consumption, wider data width and thus bandwidth, higher density, smaller form factor and lighter weight. What are preventing 3D IC integrations from High Volume Manufacturing? In this panel, the challenges on costs, business models, value chains, power distribution networks, floorplanning constraints, stacking solutions, tests, standards, ecosystem, temporary bonding and de-bonding of 3D IC integration will be discussed and some solutions are provided.



**"Challenges of Implementation of 3D Integration into Application Environment"**

Challenges for volume production in 3D integration are, for examples extended standards, flexible production lines, value chain oriented test procedures and the exchange of application experience. With improvement of these emphases we will overcome today's major barrier, the expenses of implementation and products.

***Klaus-Dieter Lang, Head of the Institute Fraunhofer - IZM***

*Professor Lang began his career as a Research Engineer at Humboldt University Berlin, where he spent 10 years (1981 to 1991) working in the areas of Microelectronic Assembly, Packaging and Quality Assurance. In 1991, he moved to SLV Hannover to build up a Department for Microelectronic and Optic Components Manufacturing. He joined Fraunhofer IZM 20 years ago and was initially responsible for R&D activities in the area of Chip Interconnection Technologies. From 2001 to 2005 he coordinated Fraunhofer IZM's Lab on Microsystem Engineering in Berlin-Adlershof, and from 2003 to 2005 he was the Head of the Department of Photonic and Power System Assembly. In 2006, he was appointed as the Deputy Director of Fraunhofer IZM, a position he held till 2010. Since 2011 he has been the Director of the Institute.*

*Professor Lang Chairs the German Chapter of IEEE-CPMT and he is a member of numerous scientific boards and conference committees. He is the author and co-author of 3 books and more than 130 publications in the field of Wire Bonding Technologies, Microelectronic Packaging, Microsystems Technologies and Chip-on-Board Technologies. He studied Electrical Engineering at the Humboldt University Berlin, and holds a Master's degree and two Doctorate degrees.*

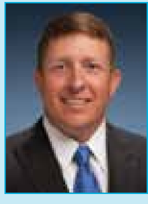
**"TSV [R]evolution: 2.5D Interposers, 3D Memory Stacks, 3D Logic on Logic"**

Adoption of TSVs in high volume applications such as wireless mobile depends on balancing value propositions more heavily weighted by cost considerations. Direct 3D TSV logic on logic stacking must also solve several key technical challenges before it will be ready for product applications, including 3D power distribution networks, floorplanning constraints, and mechanical stress management.

***Matt Nowak, Senior Director, Advanced Technology at Qualcomm***

*Matt Nowak is Senior Director of Engineering in the VLSI Technology Group of Qualcomm Technologies, Inc. His responsibilities include leadership of Advanced Technology Initiatives such as Through Silicon Stacking, Advanced Memory technology, Design for Silicon, Spintronics, and More than Moore initiatives. He manages a combination of internal advanced development teams, supplier JDPs, and consortia and university projects.*

*Matt has over 30 years of semiconductor industry experience in a variety of technical, management, and business roles including wafer fab processes and devices, CMOS ASIC technology, compound semiconductor RF devices, package design and assembly, IC design tools and methodologies, technology transfer, foundry interfacing, and advanced technology. Prior to joining Qualcomm in 2004, Matt worked for the Semiconductor Development group of Unisys/Burroughs Corporation and for the Research Laboratory of Varian Associates. He holds BS and Masters degrees in electrical engineering from Cornell University and has carried out graduate studies at Stanford University and UC San Diego. Matt is a Senior Member of the IEEE with 26 granted US patents and numerous publications and conference presentations.*



**"Challenges of 2.5D and 3D Architectures"**

2.5D and 3D architectures face a variety of challenges, most notably those around business model and ecosystem development. This panelist will focus on how Micron is addressing these challenges through the development of innovative solutions along with an ecosystem of OEMs, enablers and advanced toolset providers for their Hybrid Memory Cube.

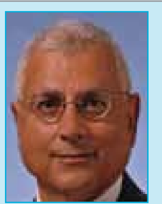
***Scott Graham, General Manager, DRAM Marketing at Micron Technology***

*Mr. Graham joined Micron in 1994 as an applications engineer in the personal computing division. He has held various managerial positions within Micron and has spent the last 11 years in Micron's memory products division, working on technical marketing for DRAM and NAND memory products. In recent years, Mr. Graham has represented Micron in various organizations responsible for setting industry standards, holding numerous vice-chair, chair, and board-level positions.*

*Mr. Graham holds a Bachelor of Science in Electronic Engineering Technology from DeVry University and a micro-MBA certification from Boise State University.*

**8:00 AM –12:00 PM**

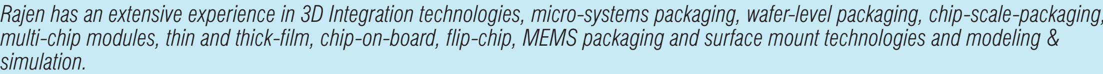
### "Temporary Bonding and Debonding Challenges"



There are several techniques to do temporary bonding/debonding, which have to be evaluated to suit a specific 3D IC process flow. With each of these techniques, a complex set of manufacturable processes/materials and equipment have to be developed. It is apparent that a large scale manufacturing requires collaboration of process, materials and equipment developers with OSATs and IDMs.

***Rajen Chanchani, Consultant (Formerly with Sandia National Laboratory)***

*Rajen Chanchani is currently a Consultant in electronic integration technologies. Prior Rajen was managing various advanced packaging and integration technologies for 32 years at Sandia National Laboratories, and at AT&T Bell Laboratories. He received his Ph.D. and M.S. in Materials Science & Engineering from the University of Florida and B. Tech. from the Indian Institute of Technology, Kanpur, India. Rajen is an IEEE Fellow, International Microelectronic and Packaging Society (IMAPS) Fellow. Rajen is also a recipient of William D. Ashman Award for his contribution to advance packaging technologies. Rajen is currently First Past-President of IMAPS.*



*Rajen has an extensive experience in 3D Integration technologies, micro-systems packaging, wafer-level packaging, chip-scale-packaging, multi-chip modules, thin and thick-film, chip-on-board, flip-chip, MEMS packaging and surface mount technologies and modeling & simulation.*

### "Status of TSV Manufacturing - Reality Check"

How far we've come, where we are, and how much further do we need to go before HVM for 2.5/3D products?" These questions will be discussed and some answers will be provided.

***Rich Rice, Sr. Vice President of Sales, ASE (US) Inc.***

*Rich Rice currently serves as Senior Vice President of Sales for ASE (U.S.) Inc., with responsibilities within the North America region. Previously, he held various engineering and business development positions at Amkor Technology and National Semiconductor Corporation. Mr. Rice serves in advisory roles for MEPTEC as well as the IMAPS Global Business Council. He holds a BS degree in Agricultural Engineering from the University of Illinois.*

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# Thursday, October 3, 2013 — Salon Rooms 1-6

| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| 1:00 PM –4:10 PM | **Technologies and Methods for 2.5/3D Packaging and Integration** *Chairs: Anwar Mohammed, John Hunt, ASE US* This session covers some emerging developments in enabling the manufacturing of 2.5/3D products. The papers cover some interesting and pertinent topics like the move of the BEOL processes towards the front end, stacking high speed memory, underfill effectiveness, reduction stepper challenges, litho optimization, IPDs and POP reliability. | **RF and Microwave Packaging** *Chairs: Xiaoguang "Leo" Liu, University of California, Davis; Fred Barlow, University of Idaho* RF and microwave applications present unique packaging challenges. This session brings together a wide range of papers on various topics including packaging for RF-MEMS, RFIC, and antennas. | **Bonding Materials and Processes** *Chairs: Maria Durham, Indium Corporation; Klaus-Dieter Lang, Fraunhofer IZM* Novel bonding materials and processes will be introduced in this session for overcoming the continuing challenges with the bonding materials and the bonding processes in various types of applications. | **LED and Optoelectronics Packaging** *Chairs: Tolga Tekin, Fraunhofer IZM; Luu Nguyen, Texas Instruments* This session will address packaging of high bandwidth optical interconnects and modules. The performance of various LED modules will also be discussed from a reliability viewpoint. | **Printed Electronics & Additive Manufacturing** *Chairs: Mike Newton, Newton Cyberfacturing; Yiliang Wu, Xerox Research Centre of Canada* Terms like the next industrial revolution have been used to describe the rapid advances in the 3D printing technology. With the convergence of additive manufacturing and printed electronics there are opportunities in the development of the next generation electronic packaging where the printed circuit board evolves into a printed circuit structure where the final produst is the package. | **Electronic Packaging for Harsh Environment Applications** *Chairs: Aicha Elshabini, University of Idaho; Tom Buschor, Harris Corporation* Extreme environment entail high temperature, extreme humidity levels, stress, and vibrations. This session addresses these issues in particular modeling and analysis of failure and design for reliability through thermal and power cycling and materials and devices selection. |
| 1:00 PM –1:25 PM | Lithography Process Optimization for 3D and 2.5D Applications *Doug Shelton, Canon U.S.A., Inc. (Tomii Kume)* | Chip Design of an 1 V RF Receiver Front-End for 5.8-GHz DSRC Applications *Wen Cheng Lai, National Taiwan University of Science and Technology (Jhin-Fang Huang, Yong-Jhen Jiangn)* | Silver Oxalate: Towards a New Solder Material for Highly Dissipative Electronic Assemblies *K. Kiryukhina, CNES (H. Le Trong, P. Tailhades, J. Lacaze, F. Courtade, S. Dareys, O. Vendier, L. Raynaud)* | Packaging of 1.3 Tbs Full Duplex Optical Interconnect *Shuki Benjamin, Compass-EOS (Kobi Hasharoni Michael Mesh)* | ***FEATURED SPEAKER*** 3D Additive Construction using Regolith *Robert Mueller, NASA Kennedy Space Center* | Advanced Devices and Packaging for Harsh Environment Operation *Aicha Elshabini, University of Idaho (Sharmin Islam, Pin-Jen Wang)* |
| 1:25 PM –1:50 PM | Integrated Passive Devices and TSV, a Disruptive Technology for Miniaturization. *Catherine Bunel, IPDIA (S. Borel, A.Lefevre, CEA-Leti, MINATEC; F. Voiron, J-R. Tenailleau, IPDIA)* | RF Device Integration on Glass Interposer toward 3D-IPAC Packages *Yoichiro Sato, Asahi Glass Company (Vijay Sukumaran, Gary Menezes, Bruce Chou, Junki Min, Motoshi Ono, Choukri Karoui, Franck Dosseul, Christian Nopper, Madhavan Swaminathan, Venky Sundaram, Rao Tummala)* | Development of low temperature sintered nano silver pastes using MO technology and resin reinforcing technology *Koji Sasaki, NAMICS Corporation (Ken Araujo, Noritsuka Mizumura)* | Preparation of a Wafer-Level Hemispherical Micro Polymer Lens Array with Improved Performance Using a Low Cost Glass Mold *Jintang SHANG, Southeast University, P.R. China (Shunjin QIN)* | A Switched-Line Microwave Phase Shifter Fabricated with Additive Manufacturing *Jonathan O'Brien, University of South Florida (Mike Newton, Thomas Weller, Daniel Silva, Eduardo Rojas)* | High Temperature Sintered Interconnects Formed by Transient Liquid Phase Sintering *Patrick McCluskey, University of Maryland CALCE* |
| 1:50 PM –2:15 PM | Frontend-ization of the Back-End *Rajiv Roy, Rudolph Technologies* | RF MEMS DPDT Switch Using Novel Simulated Seesaw Design *Mohammed Al-Amin, Anglia Ruskin University (Sufian Yousef, Barry Morris)* | Five-Layer Cu-Coated Zn/Al Clad Solder for Die Attachment *Takuto Yamaguchi, Hitachi, Ltd. (Osamu Ikeda, Shohei Hata, Yuichi Oda, Kazuma Kuroki)* | Compact Photonic Package for High-Power E-band (60-90 GHz) Photoreceiver Modules *Vitaly Rymanov, University Duisburg-Essen (Merih Palandoken, Sebastian Duelme, Tolga Tekin, Andreas Stohr)* | Fully 3D Printed 2.4 GHz Bluetooth/Wi-Fi Antenna *Paul Deffenbaugh, University of Texas at El Paso (Kenneth Church, The University of Texas El Paso; Josh Goldfarb, Xudong Chen, nScrypt, Inc.)* | Modeling of Failure in Aluminum Alloy Braze for a High Temperature Thermoelectric Assembly *Shams Arifeen, University of Idaho (Gabriel Potirniche, Aicha Elshabini, Fred Barlow)* |

**COFFEE BREAK IN FOYER: 2:15 PM – 2:30 PM — sponsored by** LORD AskUsHow™

## Thursday, October 3, 2013 — Salon Rooms 1-6

| | INTERPOSERS & 2.5/3D PACKAGING Salon 3 | MODELING, DESIGN, TEST & REL Salon 5 | MATERIALS & PROCESSES Salon 1 | ADVANCED PACKAGING & ASSEMBLY Salon 6 | ADVANCED & EMERGING TECHNOLOGIES Salon 2 | SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION Salon 4 |
|---|---|---|---|---|---|---|
| 2:30 PM –2:55 PM | Stacking of known good rebuilt wafers for high performance memory and SiP *Pascal Couderc, 3D PLUS (Jerome Noiray, Christian Val)* | | A Novel Epoxy Flux On Solder Paste For Assembling Thermally Warped POP *Ning-Cheng Lee, Indium Corporation (Ming Hu, Lee Kresge)* | A Solder Joint Reliability Model for the Philips Lumileds LUXEON Rebel LED Carrier Using Physics of Failure Methodology *Greg Caswell, DfR Solutions (Rudi Hechfellner, Michiel Kruger, Tewe Heemstra, Philips Lumileds; Nathan Blattau, Gregg Kittlesen, Vikrant More, DfR Solutions, LLC)* | Multi-layer PC Boards Fabricated using Aerosol-Jet Printing *John Bolger, Department of Defense (D.R. Hines, Laboratory for Physical Sciences, College Park; MDL. Lantz, Department of Defense; MDR. Lewis, MDR. Trudeau, KeyW Corp.)* | Thermal Evaluation of High-Current Polyimide Rigid and Rigid-Flex Printed Wiring Board Trace Widths in a Vacuum *Bennion Cannon, Honeywell (Frank Friedl, Gary Gisler)* |
| 2:55 PM –3:20 PM | A Study on the Effectiveness of Underfill in the HBM with TSV *Woong Sun Lee, SK hynix (Ho Young Son, Jin Soo Lee, Chul Gun Yoon, Min Suk Suh, Nam Seong Kim)* | | Production Proven, High Precision Temporary Bond/De-bond Process *Blake Dronen, 3M Company (Kazuta Saito, B.K. Wang)* | The Effects of Humidity and Temperature Aging Test on Flexible Packaging LED Module *ChunjinHang, Harbin Institute of Technology (Jingming Fei, WeiZhang, ChunqingWang)* | Precision Patterned Thin Films without Photolithography: Additive Manufacturing of Printed Electronics *Scott Lauer, Advantech USA* | |
| 3:20 PM –3:45 PM | Improved Compensation for a Reduction Stepper to Meet the Challenges for Advanced Packaging Applications *James Webb, Rudolph Technologies (Elvino Da Silveira, Steve Gardner, Frank Namgung)* | | Droplet-on-Demand Inkjet-filled TSVs as a Pathway to Cost-efficient Chip Stacking *Jacob Sadie, University of California, Berkeley (Niels Quack, Ming Wu, Vivek Subramanian)* | Effect of Voiding in Solder Joints on Thermal Performance of the LED *Jianbiao Pan, California Polytechnic State University* | Non-contact microwave characterization of printed resistors *Maria F. Cordoba-Erazo, University of South Florida (Thomas M. Weller)* | |
| 3:45 PM –4:10 PM | | | Microstructure and Fracture Property of Cu/In/Cu Joints in 3D Package *Yanhong Tian, Harbin Institute of Technology (Chunjin Hang, Chunqing Wang)* | Transient Thermal Analysis as In-Situ Test Method for Reliability of High Power LEDs During Temperature Cycle Tests *Gordon Elger, Technical University of Applied Science; Shri Vishnu Kandaswamy, University of Freiburg (Robert Derix, Philips Technologie GmbH; Joergen Wilde, University of Freiburg)* | | |

# Natel's First Annual Supplier of the Year Awards

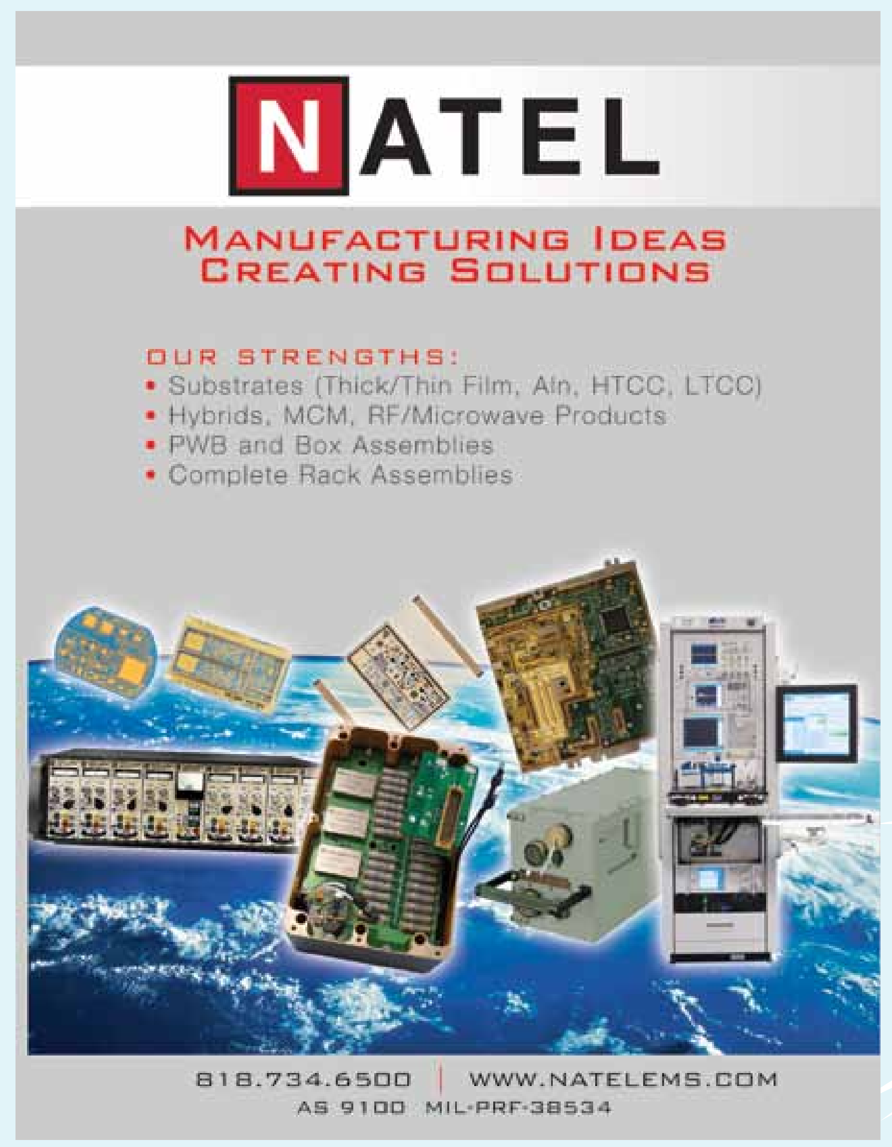
NATEL EMS will recognize 13 of its best suppliers Monday evening with its Natel supplier of the Year awards during IMAPS 46th annual International Symposium. The awards presentation will be held at the Rosen Centre Hotel in Orlando, FL during the Welcome Reception, Monday, September 30, 2013.

"The Supplier of the Year award winners represents a partnership, dedication and commitment to consistently perform above expectations. This has played an important role in Natel's success," said Sudesh Arora, President of Natel EMS. " We appreciate the efforts of these suppliers and look forward to a mutually beneficial continued relationship in the future."

The awards recognize the significant contributions of Natel suppliers as part of the company's product and performance achievement. The winners represent Natel's view, as the best the microelectronics/electronics industry has to offer in innovative technology, superior quality, outstanding launch support, crisis management and competitive total enterprise cost solutions.

The suppliers of the Year winners are chosen by the Natel team of purchasing, engineering, quality, manufacturing and logistics executives.

**The first annual awards to be given to Natel suppliers!**



# 2013 Student Symposium Programs

**Preregistration has closed. See Brian or Brianne at the registration desk for details about the tour and to meet the bus.**

Please consider participating in the IMAPS 2013 Student Programs. IMAPS leaders have designed the programs listed below to provide students with technical information, industry insight, and valuable connections. Please see more conference information at www.imaps.org/imaps2013 or contact Brianne Lamm at blamm@imaps.org for further benefits of participating.

### 2013 Student Activities Chairs:


**Venky Sundaram**
Georgia Tech University PRC
vs24@mail.gatech.edu

**Mike Newton**
Newton Cyberfacturing
mike@newtoncyberfacturing.com

**Ege Engin**
San Diego State University
aengin@mail.sdsu.edu

**Tom Weller**
University of South Florida
weller@usf.edu


### Professional Development Course (PDC) Monitor:

Students have the opportunity to serve as a PDC Monitor and attend the course free of charge. Monitor must be a full time student and are assigned on a first-come basis. Sign up early by e-mailing Brian Schieman (bschieman@imaps.org) with your top three choices no later than September 6.

### Plant Tour — Micross Components:

Micross Components will provide a valuable industry tour that will highlight two of their facilities in Orlando. Micross Components is a leading global provider of distributed and specialty electronic components for military, space, medical, and demanding industrial applications. Operating as a single source for high reliability and state of the art electronics, Micross™ solutions range from bare die and wafer processing to advanced and custom packaging to component modifications and related interconnect offerings. With a 35+ year heritage, Micross possesses the design, manufacturing and logistics expertise needed to support an application from start to finish. The plant tour is set for Wednesday, October 2: bus leaving Rosen Centre at 11:30am and returning by 2:00pm (subject to change).

***The Micross Tour is open to US Citizens ONLY. Students and industry professionals are welcome to participate. Micross will manage the approved attendee list and communicate with registrants as the tour approaches.***

### Welcome Reception:

The reception offers a good opportunity for students and advisors to talk with industry professionals in a relaxed setting to build relationships and gain valuable information..

### Student Paper Competition:

Selected student authors can deliver paper presentations that will be evaluated on technical content, presentation skills, and the written manuscript. Winning students will receive cash prizes that total $3000 and recognition in IMAPS publications.

### Student Poster Competition:

Student authors can deliver poster presentations in the University Poster Session that will be evaluated on technical content, and presentation skills. Winning students will receive cash prizes that total $500 and recognition in IMAPS publications.

### Student Chapter Booth Competition:

Highlight your academic research and programs at your student booth. Gain advice and recognition from industry leaders. Student booths will be evaluated by a panel of judges on various criteria. Winning chapter booths will receive cash prizes and IMAPS magazine recognition. Booth space is complimentary for IMAPS student members. Winning student booths will receive cash prizes that total $750 and recognition in IMAPS publications.

Please contact Brianne Lamm (blamm@imaps.org) for more information or to reserve your complimentary booth. Booth judging will be on Tuesday, October 1, 1:30 pm to 2:30 pm (Tentative).

### Employment Center:

IMAPS offer an online JOBS Marketplace for posting resumes, searching job openings, and more: http://jobs.imaps.org.

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# Orlando Area Map

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SEMINOLE COUNTY
ORANGE COUNTY
ORLANDO
LAKE BUENA VISTA
KISSIMMEE
CELEBRATION
OSCEOLA COUNTY
ST. CLOUD
MEDICAL CITY

to DAYTONA BEACH I-4 EAST
to Orlando/Sanford International Airport
to Port Canaveral, Cocoa Beach & Kennedy Space Center
TO TAMPA I-4 WEST

Semoran Blvd.
Red Bug Lake Rd.
Maitland Blvd.
Clarcona Ocoee Road
Lee Road
Aloma Ave.
University Blvd.
Fairbanks Av.
Silver Star Rd.
Princeton
Colonial Drive
Florida's Turnpike
Old Winter Garden
Curry Ford Road
Lake Underhill Rd.
Challenger Pkwy.
Conroy Rd.
Hoffner Rd.
Oak Ridge Rd.
Sand Lake Road
Beachline Expressway
Universal Blvd.
International Drive
Orangewood Blvd.
Central Florida Pkwy.
Vista Blvd.
Buena Vista Dr.
Central Florida Greeneway
Osceola Parkway
International Drive South
Boggy Creek Rd.
Irlo Bronson Memorial Highway

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BALDWIN PARK
ORLANDO SCIENCE CENTER
BOB CARR PERFORMING ARTS CENTRE
ORLANDO EXECUTIVE AIRPORT
FLORIDA CITRUS BOWL STADIUM
AMWAY CENTER
UCF ARENA
UNIVERSITY OF CENTRAL FLORIDA
THE MALL AT MILLENIA
ORLANDO PREMIUM OUTLETS - INTERNATIONAL DRIVE
FESTIVAL BAY MALL
RESTAURANT ROW
THE FLORIDA MALL
ORANGE COUNTY CONVENTION CENTER
ROSEN CENTER HOTEL
THE MAIN TERMINAL SHOPS AT OIA
ORLANDO INTERNATIONAL AIRPORT
HOSPITAL
POST OFFICE
Walt Disney World Resort
DOWNTOWN DISNEY MARKETPLACE
ORLANDO PREMIUM OUTLETS - VINELAND AVENUE
LAKE BUENA VISTA FACTORY STORES
CELEBRATION TOWN CENTER
OSCEOLA HERITAGE PARK
KISSIMMEE GATEWAY AIRPORT
Lake Tohopekaliga

# Orlando Theme Parks and Other Area Attractions

## Walt Disney World Discounted Advance Purchase Tickets

IMAPS has teamed up with Disney for a special offer for those attending IMAPS 2013 in Orlando.
Have a little fun while visiting Orlando for our 46th Symposium.

If you're planning a trip to Walt Disney World® Resort during your participation at IMAPS 2013 Orlando in September-October 2013, please visit **www.mydisneymeetings.com/imps13/** for information about ordering tickets in advance, at the special conference rate!

**Walt Disney World**
Orlando, Florida
Magic Kingdom® Park
Epcot®
Disney's Animal Kingdom®
Disney- MGM Studios

**Universal Studios**
Florida Center, Orlando, Florida
Universal Studios Florida
Universal Studios Islands of Adventure

**SeaWorld Orlando**
Orlando, Florida

**Wet 'n Wild**
Florida Center, Orlando, Florida

**Kennedy Space Center**

**Gatorland**
Orlando, Florida

**Pirate's Cove Adventure Golf**
Orlando, Florida

**Sports Dominator**
Florida Center, Orlando, Florida

**WonderWorks**
Orlando, Florida

**The Florida Mall**
Orlando, Florida

**Orange Tree Golf Club**
Orlando, Florida

**Fun Spot Action Park**
Florida Center, Orlando, Florida

**Fort Gatlin Recreational Park**
Orlando, Florida

**Bill's Airboat Adventures**
Oviedo, Florida

**Johnny's Fillin' Station Cafe**
Wadeview Park, Orlando, Florida

**Ripley's Believe It Or Not Orlando**
Orlando, Florida

**Buena Vista Watersports**
Orlando, Florida

**Harry P. Leu Gardens**
Rowena Gardens, Orlando, Florida

**Cinemark Festival Bay Mall**
Florida Center, Orlando, Florida

**Lake Buena Vista Factory Stores**
Orlando, Florida

**Long's Christian Book & Outlet**
Altamonte Springs, Florida

**Tibet-Butler Preserve**
Orlando, Florida

**Sleuths Mystery Dinner Theatre**
Orlando, Florida

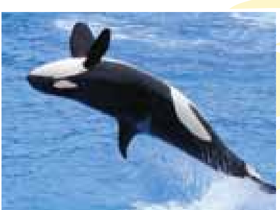
**Mennello Museum of American Folk Art**
Lake Formosa, Orlando, Florida

**Ventura Country Club Golf Course**
Ventura, Orlando, Florida

**Orlando Science Center**
Lake Formosa, Orlando, Florida

Universal Studios Florida

Gatorland

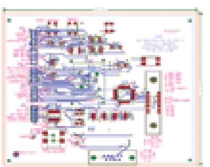
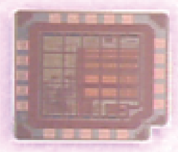


SeaWorld Orlando

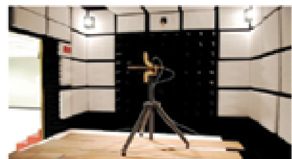
NDSU CENTER FOR NANOSCALE SCIENCE AND ENGINEERING

From Concept to Prototype
One-Stop R&D Labs

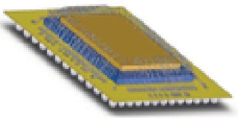
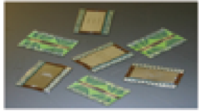
**Electronics Design, Simulation & Prototyping**
RF & digital hardware, firmware, software
System integration

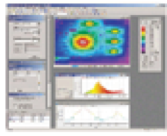
**RFID and Wireless Sensors**
Antenna simulation
Pattern measurement



**Electronics Miniaturization**
Chip scale packaging
SMT circuit board assembly

**Reliability and Failure Analysis**
Predictive modeling and reliability testing



**Microfabrication**
Thin film deposition, thick film printing
Plating. Wafer processing

Center for Nanoscale Science and Engineering
North Dakota State University
1805 NDSU Research Park Dr, Fargo ND 58102
www.ndsu.edu/cnse 701-231-5338

NDSU

# UPCOMING IMAPS EVENTS:

**Thermal Management Workshop & Tabletop Exhibition**
November 5-7, 2013 | Los Gatos, CA
www.imaps.org/thermal

**Wire Bonding Workshop & Tabletop Exhibition**
January 21-22, 2014 | San Jose, CA
www.imaps.org/wirebonding

**Global Business Council Spring Conference (GBC 2014)**
March 9-10, 2014 | Fountain Hills, AZ
www.imaps.org/gbc

**10th Device Packaging Conference & Exhibition**
March 10-13, 2014 | Fountain Hills, AZ
www.imaps.org/devicepackaging

**RF/Microwave Workshop**
April 2014 | San Diego, CA (TBD)
www.imaps.org/rf

**IMAPS New England Chapter 2014 Symposium & Expo**
May 6, 2014 | Boxborough, MA
www.imapsne.org

**HiTEC 2014 (High Temperature Electronics Conference & Exhibition)**
May 13-15, 2014 | Albuquerque, NM
www.imaps.org/hitec

**IMAPS 2014 – 47th International Symposium on Microelectronics**
October 13-16, 2014 | San Diego, CA
www.imaps2014.org

# IMAPS 2014 – San Diego

## 47th International Symposium on Microelectronics

*Bringing Together The Entire Microelectronics Supply Chain!*

**October 13-16, 2014**

**Town and Country Conference Center | San Diego, California, USA**

**www.imaps2014.org**

| Conference: | Exhibition: | Professional Development Courses: |
|---|---|---|
| **October 14-16, 2014** | **October 14-15, 2014** | **October 13, 2013** & **October 16, 2013** *(Thurs. Morning - 1/2 Day Only)* |

The 47th International Symposium on Microelectronics is being organized by the International Microelectronics Assembly and Packaging Society (IMAPS). The IMAPS Technical Committee seeks original papers that present progress on technologies throughout the entire microelectronics/packaging supply chain. The 47th Symposium on Microelectronics will feature 6 technical tracks that span the two and a half days of sessions on: ***INTERPOSERS & 2.5/3D PACKAGING; MODELING, DESIGN, TEST & RELIABILITY; MATERIALS & PROCESSES; ADVANCED PACKAGING & ASSEMBLY; ADVANCED & EMERGING TECHNOLOGIES; and SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION***, as well as an Interactive Student Poster Session.

**Technical sessions are being planned for these tracks, and abstracts will be considered on the topics listed below.** Abstracts are rated by the technical committee members and are selected into the sessions by the session chairs. Authors should identify their preferred session when submitting. Abstracts should highlight the major contributions of the work in one or more of these areas. **All abstracts submitted must represent original, previously unpublished work.**

| Track: | **INTERPOSERS & 2.5/3D PACKAGING** |
|---|---|
| Topics: | • TSV Materials & Processes • Silicon Interposers • Applications, Markets & Challenges for 2.5/3D Packaging & Integration • Glass Interposers • Technologies & Methods for 2.5/3D Packaging & Integration • Stacked Dies, Packages and Memories • 3D Simulation and Modeling • Advanced 3D Materials • PWB Embedded Device Technologies • High Density Interposers & Integrated Passives • Vertical Interconnects • Cost Considerations for 2.5/3D |
| Track: | **MODELING, DESIGN, TEST & RELIABILITY** |
| Topics: | • Design for Reliability • Modeling & Design for SI, PI and EMC • Thermal and Thermo-Mechanical Modeling • Testing Methods and Process • RF and Microwave Packaging • Mechanical Modeling and Related Metrology • Design for Manufacturing • Package Reliability Testing |
| Track: | **MATERIALS & PROCESSES** |
| Topics: | • Advanced Materials & Novel Assembly Processes • Polymers, Underfill/Encapsulants and Adhesives • Substrate Materials • Ceramic & LTCC Packaging • Bonding Materials and Processes • Embedded and Integrated Passives • Thick / Thin Films |
| Track: | **ADVANCED PACKAGING & ASSEMBLY** |
| Topics: | • Pb-Free Solder & ROHS • Wirebonding & Stud Bumping • Flip Chip Interconnects & Technologies • MEMS & Sensor Packaging • LED and Optoelectronics Packaging • Wafer Level Packaging • Chip Scale Packaging • Copper Pillar• Wafer Thinning • Wafer Bumping • Warpage Characterization and Mitigation • Integration, Mounting & Assembly of Packaged LEDs • Industry Trends & Market Drivers in Solid State Lighting • Optics & Lenses (including phosphor incorporation) • Gyros & Accelerometers • Sensors & RF Devices • Microfluidics & Bio-MEMS • Optical MEMS (MOEMS) |
| Track: | **ADVANCED & EMERGING TECHNOLOGIES** |
| Topics: | • Medical Device Packaging • Emerging Technologies • High Performance Interconnect & Boards • Printed Electronics & Additive Manufacturing • Novel Interconnections, Fabrication & Analysis Methods • Packaging for Class III Medical Implants • Human Portable Monitoring Devices • Patient Monitoring • Enabling Technologies for Power Management • Microfluidics, Bio-Sensors & Bio-Chips• Thin & Printed Battery Technology • Membrane & Capacitive Switches • Cyber Design/Cyberfacturing • Printable Display & Lighting |
| Track: | **SPECIAL SESSIONS ON PACKAGING & SYSTEM-INTEGRATION** |
| Topics: | • European Perspective • Asian Perspective • Southeast USA Perspective • Think Thin: Thin IC Packaging For Mobile Devices • Automotive, Industrial & Harsh Environment Electronics Applications • Packaging for Military Applications • Power Packaging |

Please send your 500 word abstract **electronically only** using the On-line submittal form at: www.imaps.org/abstracts.htm. **All Speakers are required to pay a reduced registration fee.** If you need assistance with the on-line submittal form, please email Brian Schieman at bschieman@imaps.org or call 412-368-1621.

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