FIVE LIVE KEYNOTES FROM INTEL, AMD, FACEBOOK, GLOBALFOUNDRIES, AND BROADCOM!

FUTURE INNOVATION FOR A CONNECTED WORLD

53rd INTERNATIONAL SYMPOSIUM ON MICROELECTRONICS
A GLOBAL VIRTUAL EVENT | OCTOBER 5-8 | IMAPS2020.ORG

- SiP/SiM / CPI (Systems Solutions)
- Wafer Level/Panel Level (Advanced RDL)
- High Performance & High Reliability

- Advanced Package (Flip Chip, 2.5D, 3D, Optical)
- Advanced Process & Materials (Enabling Technologies)

and an Interactive Poster Session

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Welcome from the General Chair

Hello IMAPS Members!

It has been a pleasure serving as this year’s General Chair for the 53rd International Symposium on Microelectronics and a privilege to be a part of such an amazing team of volunteers, speakers, and chairs. This year’s conference is virtual with the theme: **Enabling a Connected World: Always On!** The energy and innovation generated by new semiconductor products have been key enablers to the advancement of semiconductor packaging.

IMAPS 2020 offers supplementary classroom-style education in the form of two-hour short courses taught by industry leaders. We have organized this year’s live Professional Development Courses (PDCs) to be available virtually on every day of the symposium from October 2nd-October 8th. See page 6 for the listing of PDCs.

This year we have an exceptional group of committee chairs, and together with the IMAPS staff, we have assembled an excellent technical program. As our industry grows, we see a continuing trend where semiconductor products span many packaging platforms. As a result, we have maintained last year’s technical program format where the tracks are aligned by package platform to improve the attendee’s overall experience. Key package platforms include SiP/SiM/CPI, Wafer Level/Panel Level, Advanced Packaging (2.5D/3D/Flip Chip/Optical), as well as High Rel/Performance, and Advanced Process/Materials. The technical committee has put together over 75 technical presentations and posters on today’s most relevant topics in these technical tracks.

This year, we will have some highly respected industry leaders for our live Keynote talks who will set the stage for exciting virtual Plenary Sessions:

- Bryan Black, AMD
- Babak Sabi, Intel
- Ron Ho, Facebook
- Martin Weigert, Broadcom Limited
- Jeff Pauza, GlobalFoundries

Given that the symposium is virtual, the popular Posters session will be also virtual live. In addition, we invite all of you to visit and interact virtually with the exhibit booths at this year’s event. You will find a listing of the sponsors and exhibiting companies on pages 5 and 16 and at www.imaps2020.org.

This is an exciting time to be part of the microelectronics assembly and test supply chain as our industry becomes increasingly international and cross-disciplined. The advancements in connectivity continue to enhance our personal and professional lives. This, in turn, presents new challenges and opportunities for innovative solutions where the IMAPS community can experience and contribute.

**Thanks to all of you and to the Symposium Committee for making the 53rd Symposium on Microelectronics such an exciting event!** It’s been an honor and pleasure to work with my team to organize the symposium. I hope you enjoy your time attending live Keynotes, live PDCs, a live Panel Discussion, various virtual networking opportunities, and more than 75 on-demand speaker presentations at the IMAPS 2020 Virtual Conference.

Habib Hichri, PhD
Senior Fellow
Global Applications and Business Development
Ajinomoto Fine-Techno USA Corporation
General Chair, IMAPS 2020
Enabling the Future

As one of the world’s largest providers of high-quality semiconductor packaging and test services, Amkor has helped define and advance the technology landscape.

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Always On! Enabling a Connected World
## Professional Development Courses (PDCs)

Click PDC titles to view their full descriptions.

<table>
<thead>
<tr>
<th>Date/Time</th>
<th>Track A:</th>
<th>Track B:</th>
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<tr>
<td><strong>Friday, October 2</strong></td>
<td><strong>B4 – Heterogeneous Integrations (SiPs)</strong></td>
<td></td>
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<tr>
<td>9:30am-11:30am Eastern</td>
<td>John Lau, Unimicron Technology Corporation</td>
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<tr>
<td><strong>Monday, October 5</strong></td>
<td><strong>Course A3: 5G/mmWave Package Development Requirements and Solutions</strong></td>
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<tr>
<td>12pm-2pm Eastern</td>
<td>Urmi Ray, Consultant</td>
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<tr>
<td><strong>Monday, October 5</strong></td>
<td><strong>Course A4: Polymers for Electronic Packaging</strong></td>
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<tr>
<td>2pm-4pm Eastern</td>
<td>Jeffrey Gotro, InnoCentrix LLC</td>
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<tr>
<td><strong>Tuesday, October 6</strong></td>
<td><strong>Course A6: Introduction to Failure Analysis in Semiconductor Package Assembly</strong></td>
<td>Course B6: Fan Out Variations - Structures and Processes for Low and High Density</td>
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<tr>
<td>1pm-3pm Eastern</td>
<td>Tom Dory, Fujifilm Electronic Materials USA</td>
<td>John Hunt, ASE US, Inc</td>
</tr>
<tr>
<td><strong>Thursday, October 8</strong></td>
<td><strong>Course A8: The Evolution of Flip Chip Package Technology</strong></td>
<td></td>
</tr>
<tr>
<td>1pm-3pm Eastern</td>
<td>Mark Gerber, ASE US, Inc</td>
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Symposium Agenda & Keynotes

IMAPS is pleased to announce the technical program for the IMAPS 2020: Always On virtual global event. Feature presentations and PDCs will be presented live! Technical presentations will be available on-demand. Posters will be available on-demand, with a live Q&A session to complement. Learn more below!

Friday, October 2
Special early access day! Join us on this day to enjoy one-day-only sponsor and exhibitor giveaways and two live professional development courses.

9:30am-11:30am Eastern
Professional Development Courses
Separate registration fees required

Course B4: Heterogeneous Integrations (SiPs)
John Lau, Unimicron Technology Corporation

Look for these icons throughout the online program!

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Look for the announcement at IMAPS 2020

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Symposium Agenda & Keynotes

Monday, October 5
A full day devoted exclusively to professional development courses. Separate registration is required for each course. Click here to learn about all PDCs.

11am-5pm Eastern
Pre-Show SWAG Day
One day only! Log-in early for the opportunity to download swag from our sponsors and exhibitors.

12pm-2pm Eastern
Professional Development Courses
Separate registration fees required

Course A3: 5G/mmWave Package Development Requirements and Solutions
Urmi Ray, Consultant

2pm-4pm Eastern
Professional Development Courses
Separate registration fees required

Course A4: Polymers for Electronic Packaging
Jeffrey Gotro, InnoCentrix LLC

Video Space
Symposium Agenda & Keynotes

Tuesday, October 6

24hrs
Technical Presentations On-Demand
Session/speaker listing, by track, starts on page 21.

SiP/SiM/CPI (System Solutions)
Wafer Level/Panel Level (Advanced RDL)
High Performance - High Reliability
Advanced Packaging (2.5D/3D/Optical)
Advanced Processes and Materials (Enabling Technologies)

10am-3pm Eastern
Virtual Exhibit Hall LIVE Show Hours
The virtual exhibit hall is available all hours of the day through the end of October. Connect with exhibitors live during these show hours via chat and/or face to face virtual meetings.

11am-11:30am Eastern
Opening Ceremonies and Symposium Welcome Message

11:30am-12:15pm Eastern
Keynote Presentation
Advanced Packaging Architectures: Scaling for A Heterogeneous World
Babak Sabi
CVP and GM for Packaging, Assembly, and Test
Intel Corporation

Advanced Packaging Architectures are today widely acknowledged as being increasingly important to drive performance and cost improvements of microelectronics systems. As a result, several innovative packaging architectures have been announced in recent years. On-package integration provides a compact, power efficient platform for Heterogeneous Integration of diverse IP that support faster time to market and cost/yield benefits. In this talk, I will describe current technology envelopes and future scaling directions for representative advanced packaging architectures.

Key areas of focus will be (1) interconnect scaling, (2) power efficient high bandwidth signaling, (3) cost-optimized cooling and (4) advanced power delivery technologies. The talk will conclude with a call for broad collaboration across industry and academia in multiple areas including technology R&D, design, standardization and supply chain development.

Sponsored by:
12:15pm-1pm Eastern
Keynote Presentation

**Chiplets: Why AMD is Utilizing Chiplets, Some of the Challenges, and Where They May Take Us**

*Bryan Black*
Senior Fellow
AMD

Recently AMD introduced the EPYC™ server solutions which utilize Chiplets to improve performance, cost, and power. This talk will explore why AMD started using Chiplets, highlight some of the challenges, and wrap up with a discussion on where Chiplets may go and the technologies that will be required to implement future Chiplet based products.

**Sponsored by:**

1pm-3pm Eastern
Professional Development Courses
Separate registration fees required

**Course A6: Introduction to Failure Analysis in Semiconductor Package Assembly**

*Tom Dory, Fujifilm Electronic Materials USA*

**Course B6: Fan Out Variations - Structures and Processes for Low and High Density**

*John Hunt, ASE US, Inc*

1:30pm-2:30pm Eastern

**“One Year Later - What’s Changed in 2020”**

*Moderator: Priya Mukundhan, Onto Innovation*

A roundtable discussion hosted by the IMAPS Diversity and Inclusion Committee

Join Priya Mukundhan of Onto Innovation for a roundtable discussion with attendees and key conversationalists about how the events of 2020 have changed the diversity and inclusion landscape in the industry.

This session will be conducted via Zoom. Attendees are encouraged to participate in this discussion. No session pre-registration required!

**Sponsored by:**

Honeywell
3pm-4:30pm Eastern

Panel Session:

The Future Advanced Packaging Ecosystem:
Who Will Be in the Driver’s Seat?

Jan Vardaman
Chair and Moderator: E. Jan Vardaman, President, TechSearch International, Inc.

Panelists:
Koushik Banerjee, Intel Corp.
Dan Berger, GLOBALFOUNDRIES
Eelco Bergman, ASE
Mike Kelly, Amkor Technology
Khai Nguyen, NVIDIA
Craig Orr, Samsung
Ashkan Seyedi, HPE

As the industry moves to the next silicon nodes, new advanced semiconductor packaging developments are enabling the economic gains that were previously achieved with monolithic silicon scaling. Co-design of IC and package becomes increasingly important. The foundry plays an increasingly important role. Development of a healthy eco-system is critical to providing solutions to meet our industry needs. This panel will discuss the eco-system, challenges the industry faces, and the roles for the players.

Sponsored by:
Symposium Agenda & Keynotes

Wednesday, October 7

24hrs
Technical Presentations On-Demand
Session/speaker listing, by track, starts on page 21.

SiP/SiM/CPI (System Solutions)
Wafer Level/Panel Level (Advanced RDL)
High Performance - High Reliability
Advanced Packaging (2.5D/3D/Optical)
Advanced Processes and Materials (Enabling Technologies)

10am-3pm Eastern
Virtual Exhibit Hall LIVE Show Hours
The virtual exhibit hall is available all hours of the day through the end of October. Connect with exhibitors live during these show hours via chat and/or face to face virtual meetings.

11am-12pm Eastern
Keynote Presentation
Packaging Enabling Tomorrow’s Realities
Ron Ho
Director, Silicon Engineering
Facebook

Facebook’s explorations into systems for virtual and augmented reality make clear the importance of not only customized silicon hardware, but also advances in silicon packaging. In this talk we will share a vision of AR/VR and some of the computation and architectural challenges posed by AR/VR workloads and constraints.

Sponsored by:

12pm-3pm Eastern
Fraunhofer IZM & Fraunhofer USA Featured Workshop on System Integration
A live session featuring 9 speaker presentations and Q&A session.

This is a feature workshop included in full-symposium registrations! Separate registration is NOT required.
Symposium Agenda & Keynotes – Wednesday, October 7 continued

3pm-4pm Eastern
IMAPS Student-Industry Roundtable Discussion
An industry panel followed by a Q&A session for students breaking into the industry.

Join moderator Erica Folk of Northrop Grumman for an interactive discussion between industry leaders and students focused on taking the next steps into your professional career. Hear from early, mid-, and senior-level microelectronics industry professionals about what they’re looking for in new hires, how to succeed in the modern workforce, and what to expect as you progress to the next level. Come with questions and begin your networking journey!

Moderator: Erica Folk, Northrop Grumman
Panelists/Q&A Team:
Beth Keser, Intel
Mark Gerber, ASE Group
Mary Pickens, Novelis
Nicole Wongk, Honeywell
Jenny Shen, Facebook
Dan Krueger, Honeywell

Thursday, October 8th

24hrs
Technical Presentations On-Demand
Session/speaker listing, by track, starts on page 21.

SiP/SiM/CPI (System Solutions)
Wafer Level/Panel Level (Advanced RDL)
High Performance - High Reliability
Advanced Packaging (2.5D/3D/Optical)
Advanced Processes and Materials (Enabling Technologies)

10am-3pm Eastern
Virtual Exhibit Hall LIVE Show Hours
The virtual exhibit hall is available all hours of the day through the end of October. Connect with exhibitors live during these show hours via chat and/or face to face virtual meetings.
11am-12pm Eastern
Keynote Presentation

Silicon Detector Configurations for Optimizing Lidar Systems

Martin Weigert
Vice President & General Manager
Broadcom Limited

Silicon is the ideal detector material for a 905nm based Lidar System. Scalability, reliability, manufacturing capacity and well known wafer processes are clear advantages compared to III-V materials. Depending on the Lidar System approach a CMOS APD line array or a two dimensional array are possible. An interesting alternative is to use SiPMs optimized for 905nm.

Sponsored by:

12pm-12:45pm Eastern
Keynote Presentation

mmWave Antenna in Package Needs More than a Package

Jeff Pauza, Mustapha Slamani, and Selaka Bulumulla
GlobalFoundries

As the world moves towards increasing 5G mmwave connectivity, the need for cost-effective and power-efficient phased array antenna systems is amplified. This challenge can be addressed by the advantages of antenna integrated packages (AIPs). In developing antenna integrated packages (AIP), some of the factors to consider are package material properties at mmwave frequencies, design rules, heat removal method and of course, the price. Less noticeable, but still significant factors are mmwave wafer level probing and over the air testing for antenna characterization and AIP production. This presentation will discuss these factors and more to provide those considering AIP with a checklist of topics.

Sponsored by:
1pm-3pm Eastern
Professional Development Courses
Separate registration fees required

Course A8: The Evolution of Flip Chip Package Technology
Mark Gerber, ASE US, Inc.

2:30pm-5:15pm Eastern
Interactive Poster Presentations — 10 Live/1 On-Demand
Session/speaker listing, by track, starts on page 21.
Each poster presenter will be live for 15 minutes to take questions during this time.

Sponsored by:

Friday, October 9th - Friday, October 30th
This show is “Always On!” Content is archived onto the event web portal for on-demand viewing through the entire month of October.

On-Demand
Virtual Exhibit Hall
All exhibits will continue to be available for viewing during the archived period through the end of October. View and download exhibitor materials, videos, documents, and more!

Live chat and face-to-face connections will not be available during the archive period.

On-Demand
All Symposium Presentations
All content presented during the live show dates will be available on-demand in the content library during the archived period through the end of November. Catch up on or re-watch your favorite keynote addresses, the panel session, and featured live content.

Technical presentations will also remain available for on-demand viewing.

Professional development courses are live only and not available for replay after the course concludes.
Exhibiting Organizations

ASE Group
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Ajinomoto Fine-Techno USA Corp.
Canon USA
Cicor Group
Finetech
Geib Refining
Heidelberg Instruments Inc.
Heraeus Electronics
Hesse Mechatronics
IBM Canada
JIACO Instruments
Kulicke & Soffa Industries Inc.
Materion
Microcircuit Laboratories LLC
Micross
Mini-Systems, Inc.
MRSI Systems
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NorCom Systems, Inc.
NTK Technologies, Inc.
Optomec
Palomar Technologies
Plasmatreat USA
Quik-Pak
Royce Instruments
SUSS MicroTec
Specialty Coating Systems
StratEdge
Technic, Inc.
Universal Instruments Corporation

What to Expect

The IMAPS 2020 Always On! Exhibit Hall will feature virtual exhibit environments from nearly 30 industry organizations. Access to the virtual exhibit hall is INCLUDED with every full registration or a dedicated exhibit visitors pass. Learn more about registering to attend below.

Dates and Hours

October 5 | 11am EDT - 5pm EDT: Swag Day*

October 6 | 10am EDT - 3pm EDT: Virtual Exhibit Hall OPEN (LIVE show hours)

October 7 | 10am EDT - 3pm EDT: Virtual Exhibit Hall OPEN (LIVE show hours)

October 8 | 10am EDT - 3pm EDT: Virtual Exhibit Hall Open (LIVE show hours)

October 9 - October 30 | 24hrs: Virtual Exhibit Hall Open (ARCHIVED** show)

*SWAG Day is a special pre-show event! Log into the virtual event on October 5th and download swag from our exhibitors before the show officially kicks off. Swag is exclusively available on October 5th. Attendees should return for the full exhibit hall opening beginning on October 6th.

**All exhibitor environments will be archived and available for viewing throughout the month of October after the live show has ended. Learn about exhibitors, download material, view presentations, and MORE! Chat and face to face links are disabled during the archive period.
**Together as one company**, we are the only player in the semiconductor ecosystem that is offering material based solutions for **all 7 critical unit operations**.

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- **Semiconductor Packaging Dielectrics**

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info@atotech.com

<7% uniformity on RDL design
Welcome from the General Chair-elect (2021): Mak Kulkarni, Texas Instruments

Moderators: Brian Schieman, Brianne Lamm, IMAPS

**ON-DEMAND SESSION:**
U.S.-China Trade War: The Tariff Effects on the Global OSAT Market
*Stephen Rothrock, ATREG, Inc.*

**LIVE PRESENTATIONS, Thursday, October 8:**

2:30pm-2:45pm  
*New X-ray Tube Technologies for Advanced Imaging*  
Keith Bryant, KB Consulting

2:45pm-3pm  
*Gate Driver Design in 1m SiC CMOS Process for Heterogeneous Integration Inside SiC Power Module*  
Affan Abbasi, University of Arkansas

3pm-3:15pm  
*Selective Laser Sintering of Glass-ceramic Bonds Using a Defocussed ND:YAG Laser*  
Henry Lancashire, University College London  
(Murawski Karol, Aristovich Kirill)

3:15pm-3:30pm  
*The effect of Cu target pad roughness on the growth mode and void formation in electroless Cu films*  
Tobias Bernhard, Atotech Deutschland GmbH (Sebastian Zarwell, Edith Steinhäuser, Stefan Kempa, Frank Brüning)

3:30pm-3:45pm  
*Uptake Rate of Hydrogen Getter for Effectively Removing Outgassed H2 From Microelectronic Packages*  
Hua Xia, Hermetic Solutions Group (Jeffery Vriens, David DeWire)

3:45pm-4pm  
*Optimizing Industrial Soldering Processes with Digital Twins*  
Keith Perrin, Hexagon Manufacturing

4pm-4:15pm  
*Advanced Micro-structural & Thermal Modeling for Energy Generating, Wearable, Electronics*  
Keith Perrin, Hexagon Manufacturing

4:15pm-4:30pm  
*SHORT BREAK*

4:30pm-4:45pm  
*High Heat Resistant Peelable Temporary Bonding Film and New Debonding System with Xe Flash Light Irradiation*  
Yuta Akasu, Showa Denko Materials Co., Ltd.  
(Shogo Sobue, Emi Miyazawa, Tetsuya Enomoto, Takashi Kawamori, Yasuyuki Oyama, Ryoji Furutani, Yuki Nakamura)

4:45pm-5pm  
*Two-Layer Solder Resist Film with Low Young’s Modulus for High Reliability*  
YingHsuan Chou, TAIYOINK MFG. CO.,LTD.  
(Hidekazu Miyabe, Daichi Okamoto)

5pm-5:15pm  
*Package-Friendly Al2O3 Passivation Development for Cost Effect Cu Pad as Gold Replacement*  
Soojae Park, Samsung Electronics
SiP/SiM/CPI (Systems Solutions)

Track Chairs: Kim Yess, Brewer Science; Suresh Jayaraman, Amkor Technology

Technical Committee: Dev Balaraman, Wolfspeed; Karthik Dhandapani, Qualcomm; Lei Fu, AMD; Santosh Kudtarkar, Analog Devices; Fang Luo, University of Arkansas; Tarak Railkar, Qorvo; Urmi Ray, Consultant

SiP/SiM/CPI

System in Package Landscape: 2020 & Beyond
Vaibhav Trivedi, Yole Development

Solder Joint Reliability Modeling of WLP and FOWLP with Crack Path Evaluation Method under Thermal Cycling
Dae-Suk Kim, Qualcomm (Karthikeyan Dhandapani)

Thermal Improvement in 3D Embedded Modules Quantified Using Copper Bar Vias
Manoj Kakade, Psemi (Mumtaz Bora)

Lithium Battery Cell Level Fusing with Aluminum Heavy Wire Bonds
Utkarsh Mehrotra, North Carolina State University (Arthur Brazzle, Douglas Hopkins, North Carolina State University; Michael McKeown, Hesse Mechatronics)

Modeling Methodology to Quantify Impact of Package Delamination on Performance of High-Side Smart Power Switch Design
Min Chu, Texas Instruments, Inc. (Jie Chen, Abidur Rahman, Rajen Murugan)

Design Tools and Flows for the Chiplet Generation
John Park, Cadence Design Systems

Construction Kit of RF-Blocks in Package Technologies
Andy Heinig, Fraunhofer IIS/EAS

Electroplated High Performance EMI Shielding
Mustafa Oezkoek, Atotech Deutschland GmbH (Eckart Klusmann, Kuldip Johal)

Advanced No-clean Solder Paste for SIP Applications
Santosh Kumar Rath, Heraeus Materials Singapore Pte. Ltd. (Yam Lip Huei, Sylvia Sutino, Chieng Yu Yuan, Senthil Kumar Balasubramanian, Yee Ting Lo, Joel Agala, HanWen Zhang, Li-San Chan, Sungsig Kang; Sebastian Fritzsche, Heraeus Deutschland GmbH & Co. KG)

Invited Session: Heterogenous Integration Roadmap
Chair: Urmi Ray, iNEMI

HIR Overview and HIR Roadmap highlights
William Chen, ASE

5G Communications Chapter
Tim Lee, Boeing

Integrated Power Electronics Chapter
Patrick McCluskey, Univ of Maryland

Integrated Photonics Chapter
Bill Bottoms, 3MTS

Supply Chain Chapter
Tom Salmon, SEMI
TECHNICAL PROGRAM
Wafer Level/Panel Level (Advanced RDL)
TRACK CHAIRS: Beth Keser, Intel; Rey Alvarado, Qualcomm

Technical Committee: Keith Best, Onto Innovation; Tong Cui, C&B Tech; Farhad Kiaei, Dupont; Masao Tomikawa, Toray Research Center

**Advanced Packaging Technologies for High Performance Compute**
*Session Chairs: Keith Best, Onto Innovation; Masao Tomikawa, Toray Research Center*

**Heterogeneous System-In-Package (HSIP) Technology**
Charles Woychik, i3 Microsystems, Inc.
(Robert Nead, Justin Borski)

**Chip-Last, RDL-First, Fan-Out Panel-Level Packaging for Heterogeneous Integration**
John Lau, Unimicron Technology Corp. (Cheng-Ta Ko, Tony Peng, Henry Yang, Tim Xia, Bruce Lin, JJ Chen)

**Advances in Process, Materials, and Tools for FO-W/PLP**
*Session Chairs: Tong Cui, C&B Tech; Farhad Kiaei, HD Microsystems*

**Latest Technology of Epoxy Molding Compound (EMC) for FO-WLP**
Masahiro Iwai, Sumitomo Bakelite Co.,Ltd.

**6-Side Molded Panel-Level Chip Scale Package with Multiple Diced Wafers**
John Lau, Unimicron Technology Corp. (Cheng-Ta Ko, Tzvy-Jang Tseng, Tony Peng, Henry Yang, Tim Xia, Bruce Lin)

**High Frequency Dielectric Properties of Low Dk, Df Polyimides**
Masao Tomikawa, Toray Research Center
TECHNICAL PROGRAM
High Performance - High Reliability
TRACK CHAIRS: Erica Folk, Northrop Grumman; Ivan Ndip, Fraunhofer IZM

Technical Committee: Ken Kuang, Torrey Hills Tech.; Tim LeClair, Cerapax; Urmi Ray, Consultant; Zhenzhen Shen, Baker Hughes GE; Konstantin Yamnitskiy, Intel

Invited Session: Co-Design
Session Chairs: Ivan Ndip, Fraunhofer IZM; Urmi Ray, INEMI

2.5D and 3D Polyolithic Integration Technologies for Next Generation ICs
Muhammad Bakir, Georgia Tech
Co-designing/analyzing chip(let), package & board systems
John Park, Cadence Design Systems
Electrical and Photonic Networks for 2.5D Integrated Systems
Ajay Joshi, Boston University

Evaluation of System In Package implementation options in the chiplet world
Steven Watt, Zuken USA
Inductive-Coupling Wireless Bus Interface for Shape-Changeable Chiplet-Based Computers
Junichiro Kadomoto, University of Tokyo

Defense and Harsh Environment

Detecting a Security Breach and Pinpointing its Source
David Huntley, PDF Solutions

Enhancement of Board Level Reliability on Automotive DRAM Package by Optimized Thermal & Mechanical Properties
Jong Gi Lee, Samsung Electronics (Jin Soo Bae, Yeo-Hoon Yoon, Jun-Ho Lee, Kang-Young Cho)

Atomic Layer Deposition (ALD) conformal coating for robust and reliable protection of electronics and components in harsh environments
Rakesh Kumar, Specialty Coating Systems (Sawada Shuichi)

Session Sponsored by: MRSI
High Performance - High Reliability

continued

RF and Power

Electromigration in Power Devices
Hao Zhuang, Infineon Technologies (Robert Bauer, Markus Dinkel)

AE Monitoring of Fatigue Damage of Al Ribbon Bonding for Power Electronic Devices During Power Cycling Test
Katsuaki Suganuma, Osaka University (Chanyang Choe, Chuantong Chen)

Enhancement of ESD Performances of Silicon Capacitors for RFID Solutions
Sebastien Jacqueline, Murata (Catherine Bunel, Laurent Lengignon)

Wireless Sensor Platform for Nanosensor Interface Electronics
Bruce Kim, City University of New York

Reliability Modeling, Simulation and Testing

Reliability Simulation of Cu/Polymer interface in Fan-out Wafer Level Packaging
Yuji Okada, ASAHI KASEI Corporation (Atsushi Fujii, Yoshiharu Kariya, Kenta Ono)

Acceleration Factors and Life Predictions
Greg Caswell, ANSYS, Inc. (Chris South)
TECHNICAL PROGRAM

Advanced Packaging (Flip Chip/2.5D/3D/Optical)

TRACK CHAIRS: Sandeep Sane, Intel; Frank Eberle, Northrop Grumman; Jaimal Williamson, Texas Instruments

Technical Committee: Manish Dubey, Intel; Dan Krueger, Honeywell; Shubhada Sahasrabudhe, Intel; Tolga Tekin, Fraunhofer IZM; Jim Will, Micross

Advanced Die-Beam alignment method for Laser-Assisted Bonding
Wagno Alves Braganca Jr., JCET STATSChipPAC Korea (KyungOe Kim)

Characterization of sintered Cu Nanopaste for micro-bumping with Injection Molded Solder Technology
Toyohiro Aoki, IBM Research Tokyo (Eiji Nakamura, Sayuri Kohara, Chinami Marushima, Kuniaki Sueoka, Takashi Hisada, Ryota Yamaguchi)

Flip Chip

Simulation and Experimental Study on IMS (Injection Molded Solder) Bumping with Expanded Resist Patterning for Reinforcement of Fine-pitch Capability
Risa Miyazawa, IBM Research Tokyo (Eiji Nakamura, Toyohiro Aoki, Chinami Marushima, Takashi Hisada)

Ultra-low residue Flux Application in RF Front End Package
Leo Hu, Indium Corporation

Heterogeneous Integration & 3D

A Novel Approach to Mitigate Stress Induced Defects at Metal-Dielectric Interface in RDL for 3D IC Stacking
Amit Kumar, Bridging the Innovation Development Gap (BRIDG) (Jose Chacon, Peter Gelzinis)

Hybrid Bonding of Via-middle TSV Wafer Fabricated Using Direct Si/Cu Grinding, Residual Metal Removal, CVD and CMP
Naoya Watanabe, AIST (Hirosi Yamamoto, Takahiko Mitsui, Eiichi Yamamoto)

Evaluating Thermoset Resin Substrates for 3D Mechatronic Integrated Devices and Packaging
Felix Haeussler, Institute for Factory Automation and Production Systems (Simon Pettillon, Johannes Dornheim, Shengxia Shen, Wolfgang Eberhardt, André Zimmermann, Jörg Franke)

Challenges in Placement Requirements for System in Package Integration
Chan Pin Chong, Kulicke & Soffa

DuPont(TM) GreenTape(TM) LTCC Materials for Wireless Electronic Devices
Brian Laughlin, DuPont Microcircuit Materials (Mark Easton, Kaylan Rapolu, Ken Souders, ChunAn Lu)

Ultra-thin Flip Chip Assembly for Heterogenous and Hybrid Integration
Douglas Hackler, American Semiconductor, Inc.

Interconnect

Optimization of High-Speed Electrolytic Plating of Copper Pillar to Achieve a Flat Top Morphology and Height Uniformity
Ikumoto Raihei, C.Uyemura & Co., Ltd.

Methods to Reduce the Hierarchy of Interconnections in Electronic System
Dyf-Chung Hu, SiPlus Co.

Printed Interconnects & RF Devices for High Frequency Applications
Bryan Germann, Optomec

Parameter Optimization for Unstable Pin Bonding
Henri Seppanen, Kulicke & Soffa

continued
Technical Program

Advanced Packaging (Flip Chip/2.5D/3D/Optical)

Optical

Optimizing Package Yield and Reliability with X-ray Inspection
Sudhakar Raman, SVXR, Inc. (Michael Kwan, Rhiannon Brooks, Andrew Reid, Fred Duewer)

Optical Data Link Module for Data Transmission in Smart Catheters
Jian Li, Delft University of Technology (Vincent Hennenken, Marcus Louwere, Ronald Dekker)

Control of Advanced Packaging by Improved Optical Profiler Metrology
Samuel Lesko, Bruke

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Technical Program

TECHNICAL PROGRAM
Advanced Process & Materials (Enabling Technologies)
TRACK CHAIRS: Benson Chan, Binghamton University; Mark Hoffmeyer, IBM

Technical Committee:
Doug Shelton, Canon; Kevin Demartini, DuPont; Jeff Gotro, Innocentrix;
Douglas C Hopkins, NCSU; Michael McKeown, Hesse Mechatronics; Sylvain Pharand, IBM;
Martin Schneider-Ramelow, Fraunhofer IZM; Aric Shorey, Mosaic Microsystems;

Electroless Plating with UV Modification for Thermosetting Dielectric and Decay Suppression of High Frequency Transmission Property
Masaya Toba, Showa Denko Materials Co., Ltd. (Kazuyuki Mitsukura, Masaki Yamaguchi)

Packaging Issues and Solutions for Ultra-Low Power, High Efficiency GaN micro-LEDs for Battery Free, Sub-mm2, Smart IoT Systems
Frank Libsch, IBM T.J. Watson Research Center (Steve Bedell, Bucknell Webb, Arun Paidimarri)

Additive Manufacturing
A Novel Method for Characterization of Ultra Low Viscosity NCF Layers Using TCB for 3D Assembly
Giovanni Capuz, IMEC (Melina Lofran, Carine Gerets, Fabrice Duval, Pieter Bex, Jaber Derakhshandeh, Alain Phommahaxay)

Advanced Substrates
Thin Glass Handling Solutions for Microelectronics Packaging
Aric Shorey, Mosaic Microsystems (Shelby Nelson, David Levy, Paul Ballentine)

Plasma Surface Engineering: An Enabling Technology Designed to Clean and Protect Printed Circuit Boards
Daphne Pappas, Plasmatreat USA (Sebastian Guist, Dhia Ben Salem, Plasmatreat GmbH)

Advanced Low Df Dry film Build-up Material on Glass Panel for 5G Application
Takenori Kakutani, TAIYO INK MFG. CO., LTD. (Zhong Guan, Yuya Suzuki, TAIYO INK MFG. CO., LTD.; Ali Muhammad, Serhat Erdogan, Atom Watanabe, Mohanalingam Kathaperumal, Madhavan Swaminathan, Georgia Institute of Technology)

Electrical Performance and Robustness of Ultrathin High-Density Carbon Nanofiber Capacitors on Silicon, Alumina and Glass Substrate Materials
Victor Marknäs, Smoltek AB (Vincent Desmaris, Amin M Saleem, Maria Bylund, Ricakrd Andersson, Elisa Passalacqua, Mohammed Shafiq Kabir)

Development of Dielectric Material Enabling Low Insertion Loss of Organic Substrates at Various Operational Temperatures
Tatsushi Hayashi, Sekisui Chemical Co., Ltd. (Watanabe Ryoichi, Lin Po Yu, Ichikawa Seiko)

continued
Wire Bond & Advanced Interconnect

Cell Interconnections in Battery Packs Using Laser-assisted Ultrasonic Wire Bonding
Andreas Unger, Hesse Mechatronics (Matthias Hunstig, Michael Brökelmann, Dirk Siepe, Hans Hesse)

Evaluation of High Melting Point Lead-free Solder and Hybrid Sinter Paste as Attaching Material for Clip Bond Package
Fred Fuliang Le, Nexperia (Rinse van der Meulen, Yoon Kheong Leong, Manoj Balakrishnan, Zunyu Guan)

An Oxide Wear Model of Ultrasonic Ball Bonding
Brandon van Gogh, Santa Clara University (Tioga Benner, Calvin Tseng, Panthea Sepehrband, Santa Clara University; Henri Seppaenen, Kulicke & Soffa Industries, Inc.)

Wire Bonding: The Ultrasonic Bonding Mechanism
Lee Levine, Process Solutions Consulting

Wire-Bonding Reliability Evaluation
Hossein Akbari, Schlumberger

Thermal

Thermal Management in High-Density High-Power Electronics Modules Using Thermal Pyrolytic Graphite
Riya Paul, University of Arkansas (Amol Deshpande, Fang Luo)

Novel TIM Solution with Chain Network Solder Composite
Ning-Cheng Lee, Indium Corporation (Runsheng Mao, Sihai Chen, Elaina Zito, Dave Bedner)

Characterization of Highly Thermally Conductive Organic Substrates for a Double-Sided Cooled Power Module
Tzu-Hsuan Cheng, NC State University (Utkarsh Mehrotra, Karan Maru, B. Jayant Baliga, Subhashish Bhattacharya, Douglas Hopkins)

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