FINAL PROGRAM

54th INTERNATIONAL SYMPOSIUM on MICROELECTRONICS
OCTOBER 11-14, 2021 • SAN DIEGO, CA • IMAPS2021.org

Conference: October 12-14, 2021
Exhibition: October 12-13, 2021
Professional Development Courses: October 11, 2021

General Chair: Mak Kulkarni
Texas Instruments

General Chair-elect (2022): Sandeep Sane
Intel Corporation

Past General Chair (2020): Habib Hichri
Ajinomoto Fine-Techno USA

See page 7 for the
DIVERSITY & INCLUSION TOWNHALL DISCUSSION:
Career Growth During a Global Pandemic

Sponsored by: Honeywell
The SiP Company

Innovative IC, SiP, and MEMS packaging portfolio to serve dynamic mobility, IoT, high performance computing, automotive and AI markets.

PoP • Flip Chip • SiP • WLP • Fanout • FOCoS
2.5D • TSV • Flex • AoP • AiP • Shielding
Wire Bond • Embedded • Substrate • Co-Design

Package it.
“Welcome Back. Face To Face.” This tag line may be a bit surprising, but it’s true. We are excited about the opportunity to see old faces and meet new ones - in person - and learn about the latest advances and future plans in microelectronics packaging technology from the experts in the industry at IMAPS 2021! The pandemic is not over yet, neither in the US nor in many parts of the world, but we are taking advantage of the fact that we now have the knowledge and the procedures in place to safely gather for such events.

It is my pleasure to serve as the General Chair for the 54th International Symposium on Microelectronics. It has been a rewarding journey this year working alongside a great team of volunteers and staff to organize a very educational program and a set of events to facilitate exchange of ideas spanning a wide range of topics in the entire microelectronics packaging supply chain. This annual event provides an excellent opportunity to network with professionals in the microelectronics packaging/assembly/test fields across the globe.

As always, IMAPS 2021 offers supplementary classroom-style education in the form of two-hour short courses (PDCs) taught by industry leaders. In addition, we have 50 booths with exhibits from a wide range of companies involved in the packaging supply chain.

This year, we have exceptional industry leaders for our keynote talks, such as Dr. Hamid Azimi of Intel, Dr. Suresh Ramalingam of Xilinx, Mr. KT Moore of Cadence, Dr. Roman Ostholt of LPKF, Dr. Peter O’Brien of Tyndall Institute, and Mr. Jean-Christophe Eloy of Yole Développement. They will give their perspectives on ongoing as well as expected advances in various areas of packaging technology. In addition, Jan Vardaman of TechSearch International will lead a panel discussion with a team of experts to answer the question “Next Generation Packages: Are We Ready?”

We have a great team of technical committee chairs along with the IMAPS staff that has put together an excellent technical program in the form of presentations, papers, and posters in various fields of packaging such as Heterogeneous Integration, Manufacturing Optimization, Wafer Level/Panel Level, High Performance, High Reliability, Flipchip/2.5D/3D, Optical, and Advanced Process and Materials. These more than 100 presentations are a combination of peer reviewed submissions as well as invited talks.

Opportunities and challenges posed by the demands on the electronics assembly and test supply chain are increasing rapidly due to the wide range of applications in Communications (5G), High Performance Computations, Automotive, Industrial, Medical, Defense/Space, and many other industries. IMAPS 2021 hopes to help the community come together and take on these challenges by exchanging the knowhow and the ideas. Looking forward to seeing you all!

You can participate in-person or virtually in 2021

**In Person**
- Live Keynote, Panel, HIR Workshop, PDCs and Posters
- Exhibit Hall access
- Breakfast and lunch each day along with receptions in the Exhibit Hall
- On Demand access for all Keynote, Panel, HIR Workshop, and Posters

**Virtually**
- On Demand access for Keynote, Panel, HIR Workshop, and Posters
- Live stream access to PDCs

NOTE: PDCs are an additional fee.

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IMAPS 2021 Sponsors

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We are planning a safe and successful event to welcome you back in-person to IMAPS 2021 San Diego!

Your Symposium experience will look and feel a little different than you remember. The safety and well-being of our attendees is a top priority so we will follow the many recommended safety protocols below.

TOGETHER, we can ensure a safe and successful IMAPS 2021!

- IMAPS is consulting government agencies, event partners, and our stakeholders regarding the Covid-19 virus ahead of IMAPS 2021 San Diego. IMAPS leadership will keep attendees informed of any impact to the event. IMAPS remains committed to delivering the best Symposium this Fall and anticipates a robust, healthy event for all of our attendees, speakers, and exhibitors. IMAPS is prepared for all options for alternative conference plans in the event that the in-person components of the Symposium are deemed unsafe or not possible.

- Following CDC and California Department of Public Health guidelines for our event size, attendees are NOT required to provide vaccination records or COVID-19 test results.

- IMAPS strongly recommends that MASKS be worn by all attendees at all times during any indoor IMAPS 2021 functions (session rooms, exhibit hall, registration area, etc.).

- Per San Diego County guidelines, the following are exempt from wearing masks at all times: People with a medical condition, mental health condition, or disability that prevents wearing a mask. People who are hearing impaired, or communicating with a person who is hearing impaired, where the ability to see the mouth is essential for communication.

- IMAPS recommends that all attendees bring their own masks.

- IMAPS and the Town & Country Hotel will make masks available.

- IMAPS requests that you pre-register online immediately to allow our staff adequate time to properly prepare space requirements.

- **Please do not attend in-person if you do not feel well or are showing Covid symptoms, rely on virtual participation.**

- Follow local health guidance.

- Wash your hands frequently. Please avoid handshaking, touching, close proximity, etc.

- Be mindful and respectful of other attendees’ comfort levels.

- Hand Sanitizer will be available outside every meeting room, restaurant, lobby, etc.

- IMAPS will also provide additional hand sanitizer.

- IMAPS organizers will be following CDC guidelines, as well as locally enforced restrictions, on seating capacity and social distancing. Meeting and banquet arrangements are set to allow for physical distancing between attendees including conference and table seating.

- Self-serve banquet-style food service has been suspended and replaced by alternative service styles including plated meals and pre-packaged grab and go dining options, with single-use condiments, as well as full-service coffee and refreshment.

- IMAPS will attempt to hold receptions and non-technical meetings outdoors, if possible.

- The health and wellness of our group attendees are paramount at Town and Country Resort.

  » The entire resort, including our meeting rooms, is deep cleaned and thoroughly sanitized regularly using Victory Innovations electrostatic disinfectant sprayers containing Bioesque hospital-grade disinfectant.

  » Guests care items are available upon request including disposable masks and gloves.

  » Read about the Town & Country’s efforts to ensure a safe and comfortable experience during your stay.
COVID-19 Safety Acknowledgment – Liability Waiver and Release of Claims

All attendees at the 54th International Symposium on Microelectronics, in consideration of being permitted to attend:

(1) Acknowledge that:
• There is a risk of contracting COVID, even for persons who are vaccinated against COVID.
• There may be others in attendance who are not vaccinated against COVID.
• COVID can cause serious illness with lingering effects, and even death.
• No amount or extent of precautions can guarantee against contracting COVID.

(2) Knowingly and voluntarily assume all risk of injury, harm, and loss, and even death, associated with attendance at the 54th International Symposium on Microelectronics, exposure to COVID, and contracting COVID.

(3) RELEASE, WAIVE AND FOREVER DISCHARGE ANY AND ALL LIABILITY, CLAIMS, AND DEMANDS OF WHATEVER KIND OR NATURE AGAINST IMAPS, ITS DIRECTORS, OFFICERS, EMPLOYEES, VOLUNTEERS, AND AGENTS (THE “RELEASED PARTIES”), IN LAW AND IN EQUITY, TO THE FULLEST EXTENT PERMISSIBLE BY LAW, INCLUDING BUT NOT LIMITED TO DAMAGES OR LOSSES CAUSED BY THE NEGLIGENCE, FAULT OR CONDUCT OF ANY KIND ON THE PART OF THE RELEASED PARTIES, INCLUDING BUT NOT LIMITED TO DEATH, BODILY INJURY, ILLNESS, ECONOMIC LOSS OR OUT OF POCKET EXPENSES, OR LOSS OR DAMAGE TO PROPERTY, WHICH ARISE FROM MY PARTICIPATION ATTENDANCE AT THE 54TH INTERNATIONAL SYMPOSIUM ON MICROELECTRONICS, INCLUDING DUE TO COVID.
## Technical Program
### Professional Development Courses (PDCs):

**All PDCs held Monday, October 11, 2021**

**7:00 AM - 5:30 PM**

<table>
<thead>
<tr>
<th>Time</th>
<th>Course Description</th>
<th>Instructor(s)</th>
<th>Location</th>
<th>Virtual Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>8:00 am - 10:00 am</td>
<td>System-in-Package (SiP) - System Solutions Through Miniaturization</td>
<td>Mark Gerber, ASE US, Inc.</td>
<td>IN-PERSON Room: PALM 1</td>
<td>Remote attendees can connect</td>
</tr>
<tr>
<td>10:00 am - 10:30 am</td>
<td>PDC Coffee Break</td>
<td></td>
<td>PALM ROOM 4</td>
<td></td>
</tr>
<tr>
<td>10:30 am - 12:30 pm</td>
<td>Advances in Fan-Out Wafer-Level Packaging</td>
<td>Beth Keser, Intel Corporation</td>
<td>IN-PERSON Room: PALM 1</td>
<td>NO Remote attendees</td>
</tr>
<tr>
<td>12:30 pm - 1:00 pm</td>
<td>PDC “Box Lunch” for those taking morning &amp; afternoon classes</td>
<td></td>
<td>PALM ROOM 4</td>
<td></td>
</tr>
<tr>
<td>1:00 pm - 3:00 pm</td>
<td>The Evolution of Flip Chip Package Technology</td>
<td>Mark Gerber, ASE US, Inc.</td>
<td>IN-PERSON Room: PALM 1</td>
<td>Remote attendees can connect</td>
</tr>
<tr>
<td>3:00 pm - 3:30 pm</td>
<td>PDC Coffee Break in Foyer</td>
<td></td>
<td>PALM ROOM 4</td>
<td></td>
</tr>
<tr>
<td>3:30 pm - 5:30 pm</td>
<td>Fan-out Wafer/Panel-level Packaging</td>
<td>John Lau, Unimicron Technology Corp.</td>
<td>IN-PERSON Room: PALM 1</td>
<td>Remote attendees can connect</td>
</tr>
<tr>
<td>5:30 pm - 7:00 pm</td>
<td>WELCOME RECEPTION</td>
<td></td>
<td>FLAMINGO LAWN (Outside – weather permitting)</td>
<td>Sponsored by: ASE GROUP</td>
</tr>
</tbody>
</table>

**Registration Open**

IMAPS Registration (T&C Foyer)

**IMAPS 2021 • 54th Annual Symposium on Microelectronics**
Monday, October 11, 2021...continued

7:00 pm – 8:00 pm
DIVERSITY & INCLUSION TOWNHALL DISCUSSION:
Career Growth During a Global Pandemic
PALM ROOMS 5-6

Sponsored by: Honeywell

Moderator/Chair: Erica Folk, Northrop Grumman
Townhall Participants: Beth Keser, Intel Corp.; Mak Kulkarni, Texas Instruments; Marqus Patton, SD National Society of Black Engineers; Nicole Wongk, Honeywell

This will be a one-hour townhall – open discussion and “panel” format. Join us for open and lively conversation around many important topics for all to consider in today’s challenging pandemic work environment, including:

The importance of diversity within IMAPS Diversity in Challenges in a virtual workplace Best practices for diversity and inclusion How to make an impact in your workplace And more...

Look for these icons throughout the program!

Access the IMAPS 2021 MOBILE APP

Conference App Sponsored By cadence®

The mobile app is the exclusive source for all speaker presentations

PLUS
● The full conference program
● Session descriptions
● Searchable attendee list
● Searchable exhibitor list
● Info, Links, and News
● Conference updates and
● Personal conference schedule
● Live Streaming & On-demand presentations
● Exhibitor Lead Retrieval

Download to access streams / on-demand!

1. Visit the Apple Store or the Google Play store and search “IMAPS Events” or visit https://imaps.gatherdigital.com for the web-based version.
2. Log in with your registration email and the password imaps2021.
3. Take advantage of all of the attendee and exhibitor features!
In-Person / Live Program Agenda

Tuesday, October 12, 2021

7:00 AM – 5:30 PM  Registration Open
IMAPS Registration (T&C Foyer)

11:00 AM – 4:30 PM  Exhibit Hall Open
IMAPS Exhibit Hall (Golden State Ballroom)

7:30 AM – 8:30 AM  Breakfast & Coffee in Foyer
IMAPS Registration (T&C Foyer)

Sponsored by

IMAPS 2021 Opening Plenary Session & Keynotes:
8:30 AM - 11:30 AM:

IN-PERSON
Room: Town & Country A
Streaming - Remote speakers & attendees can connect

Sponsored by:

IMAPS Business Meeting, Awards, Exec Council, etc. – Rich Rice, Beth Keser, Ron Huemoeller, IMAPS Presidents – Mak Kulkarni, General Chair

Introduced by General Chair...
9:00 AM – 9:45 AM: Keynote 1:

Keynote Presentation 1:  VIRTUAL PRESENTATION
ADVANCED PACKAGING ARCHITECTURES: OPPORTUNITIES AND CHALLENGES

Advanced packaging architectures are today widely acknowledged as being increasingly important to drive performance and cost improvements of microelectronics systems. As a result, several innovative packaging architectures have been announced in recent years. On-package integration provides a compact, power efficient platform for Heterogeneous Integration of diverse IP that support faster time to market and cost/yield benefits. In this talk, I will describe current technology envelopes and future scaling directions for representative advanced packaging architectures. Key areas of focus will be (1) interconnect scaling, (2) power efficient high bandwidth signaling including optical interconnects, (3) Hybrid Bonding, (4) test challenges for chiplets/die block assembly, and (5) advanced power delivery technologies. The talk will conclude with a call for broad collaboration across industry and academia in multiple areas including technology R&D, design, standardization and supply chain development.

Hamid Azimi, Ph.D., Intel Corporation
Corporate Vice President, Director, Substrate Packaging Technology Development

Dr Azimi leads substrate package technology development organization at Intel and is responsible for developing industry leading substrate packaging materials, processes, and equipment technologies as well as the associated supply chain capabilities to enable high volume manufacturing for substrates across our 15+ supplier factories. He joined Intel in 1995 and has since served in various leadership roles in Technology Development Organization. Starting 2010, he led the establishment of Intel’s first substrate R&D factory in Chandler AZ which became the birthplace of panel level die embedding (EMIB) and the key corner stone for establishing package platforms for Intel data center products. Hamid holds more than a dozen patents and has given numerous talks at international conferences. He is a board member and the General Chair of International Semiconductor Executive Summit. In 2014, Hamid received Distinguished Alumni Award from Lehigh University where he completed his PhD in materials Science and engineering.
Achieve Better System-Level PPA with Heterogeneous, Multi-Chiplet Packaging
YOU CAN SUPPORT NATIONAL SECURITY

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Honeywell is dedicated to support our national security mission at the U.S. Department of Energy’s Kansas City National Security Campus. With more than 5,500 employees, we are devoted to providing our people a workplace that feels inclusive and rewarding to all. Join us in pioneering new technologies and advanced solutions!

kcnsd.doe.gov/careers

THE FUTURE IS WHAT WE MAKE IT | Honeywell
9:45 AM – 10:15 AM: Coffee Break in Foyer
IMAPS Registration (T&C Foyer)

Sponsored by:

9:45 AM – 10:15 AM: Coffee Break in Foyer
IMAPS Registration (T&C Foyer)

10:15 AM – 11:00 AM: Keynote 2:

Keynote Presentation 2:
MORE MOORE OR MORE THAN MOORE. AN EDA PERSPECTIVE

Over the past 30+ years there’s been a significant shift in the way commercial electronics have been designed. There are many inflection points that have influenced how consumer electronics and systems products are developed across many vertical markets including transportation, 5G, wireless communications, industrial, medical, and more. This talk will discuss the impact several drivers including Moore’s Law, as well as advances in the design of semiconductors, systems, and advance packaging.

KT Moore, Cadence Design Systems, Inc.
Vice President
KT Moore joined Cadence in August 2012 and is currently responsible for business development and product marketing for the CPG covering Cadence’s full suite of custom IC, PCB, and Systems Analysis products. This encompasses several key technology areas including custom IC layout and automation, circuit level simulation, PCB design, and multi-physics analysis and simulation. Prior to joining Cadence, KT spent 12 years with Magma Design Automation. During that time he served 6 years as a Global Account Director, and 6 years as a Vice President of Product Marketing, where he was responsible for business development and marketing for all Magma products. Before joining Magma KT also held various sales positions with EPIC Design Technology and Valid Logic Systems. Prior to his career in EDA, KT spent several years as a logic designer for Texas Instruments. KT received a Bachelor of Science degree in Electrical Engineering and Applied Physics from Case Western Reserve University in Cleveland, OH in 1985.

11:00 AM - 11:15 AM: Thank you and wrap-up by General Chair

11:15 AM – 1:15 PM: Networking & Lunch in Exhibit Hall
IMAPS Exhibit Hall (Golden State Ballroom)

Sponsored by:

ASE GROUP
### 1:15 PM – 5:50 PM: Tuesday Afternoon Technical Sessions

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<th>TRACK 2</th>
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<td>1:15 PM - 4:30 PM</td>
<td>Hi-Rel Session 1: HIGH RELIABILITY PACKAGING, RF, DESIGN</td>
<td>Materials Session 1: NOVEL FABRICATION METHODS</td>
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<tr>
<td></td>
<td>Session Chairs: Tim LeClair, Cerapax</td>
<td>Session Chairs: Kevin Demartini, DuPont</td>
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<td></td>
<td>Ken Kuang, Torrey Hills Tech.</td>
<td>Jeff Gotro, Innocentrix</td>
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<td>Room: Town &amp; Country A</td>
<td>Room: Town &amp; Country B</td>
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<tr>
<td></td>
<td>No Streaming – All in-person</td>
<td>No Streaming – All in-person</td>
</tr>
<tr>
<td>1:15 PM - 1:40 PM</td>
<td>Design Benefits of Coaxial TGV Substrates, Enhancing RF Via to Via Isolation</td>
<td>Directed Assembly-based High-throughput Printing of Nano &amp; Microelectronics and Interposers</td>
</tr>
<tr>
<td></td>
<td>Tim LeClair, Cerapax (Steven Martin)</td>
<td>Ahmed Busnaina, Northeastern University</td>
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<tr>
<td>1:45 PM - 2:10 PM</td>
<td>Capacitors for Energy Storage and as a Companion to WBG Development</td>
<td>Fabrication of Printed and Nanostructured Breath Sensor Arrays</td>
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<td></td>
<td>Roger Brewer, Lockheed Martin</td>
<td>Guojun Shang, Binghamton University (Dong Dinh, Shan Wang, Behnaz Malaei, Courtney Fu, Shan Yan)</td>
</tr>
<tr>
<td>2:15 PM - 2:40 PM</td>
<td>High Frequency, Low Loss, Additively Manufactured Hermetic Package</td>
<td>Digital, Multi-Materials, Non-Contact Large Area Printer</td>
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<td>Timothy Smith, Cubic-Nuvotronics</td>
<td>Ralph Birnbaum, IO Tech (Guy Nesher, Herve Javice, Michael Zenou)</td>
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<tr>
<td>2:45 PM - 3:10 PM</td>
<td>New approach for High Reliable &amp; Cost-Effective Solder alloys for</td>
<td>Fabricating Micro/Nano electrode Arrays for Integrating into</td>
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<td>Automotive Applications</td>
<td>Wearable Sensors and Electronics</td>
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<tr>
<td></td>
<td>Sebastian Fritzche, Heraeus Deutschland GmbH &amp; Co. (Michael Joerger,</td>
<td>Shan Wang, Binghamton University (Guojun Shang, Justine Gordon, Nina Filipponea, Richard Robinson, Mark Schadt, Chuanjian Zhong)</td>
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<td></td>
<td>Manu Noe Vaidya, Peter Prenosil, Katja Stenger, Joerg Trodler)</td>
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<tr>
<td>3:15 PM - 3:40 PM</td>
<td>Thin Film Flexible Circuits with Embedded ASICs; Enabling Technology</td>
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<td>for Sophisticated Medical Applications</td>
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<td></td>
<td>Alexander Kaiser, Cicor Group (Rick Elbert)</td>
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<td>3:40 PM - 4:30 PM</td>
<td>Break in Exhibit Hall</td>
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<td>IMAPS Exhibit Hall (Golden State Ballroom)</td>
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<td></td>
<td>Amkor Technology</td>
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<tr>
<td>4:30 PM - 5:55 PM</td>
<td>Advanced Packaging Session 1: FLIP CHIP</td>
<td>Wafer Level Session 1: WAFER-LEVEL FAN OUT &amp; ADVANCE RDL</td>
</tr>
<tr>
<td></td>
<td>Session Chair: Frank Eberle, Northrop Grumman Corp.</td>
<td>Session Chair: Irene Popova, Ancosys</td>
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<td>Room: Town &amp; Country A</td>
<td>Room: Town &amp; Country B</td>
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<tr>
<td></td>
<td>No Streaming – All in-person</td>
<td>No Streaming – All in-person</td>
</tr>
<tr>
<td>4:30 PM - 4:55 PM</td>
<td>An Investigation of Thermomigration Failure of Flip Chip Solder Joint Interconnects in High Reliability Applications</td>
<td>Fine Line and Low Stress RDL Solution for Fan-out Wafer Level &amp; Panel Level Packaging</td>
</tr>
<tr>
<td></td>
<td>Aimee Morey, CAES (Scott Popelar, Julie Hook)</td>
<td>Yoshinori Matsuura, Mitsui Mining &amp; Smelting Co. Ltd. (Joji Fujii)</td>
</tr>
<tr>
<td>5:00 PM - 5:25 PM</td>
<td>Ultra wide-band, Low Loss RF Substrate with High-density DC Routing Supporting 5G/6G Flip-chip RFICs</td>
<td>Novel Lithography Technology of Enhancing Resolution Limit with the Lithography and Plating Process</td>
</tr>
<tr>
<td></td>
<td>Timothy Smith, Cubic-Nuvotronics</td>
<td>Hiroshi Matsui, Independent Researcher and Inventor</td>
</tr>
<tr>
<td>5:30 PM - 5:55 PM</td>
<td>Memory Packaging Challenges for a Growing Market</td>
<td></td>
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<td></td>
<td>Knowlton Olmstead, Amkor Technology, Inc. (Curtis Zwenger, Richard Strode)</td>
<td></td>
</tr>
</tbody>
</table>
5:30 PM – 7:00 PM: Posters & Pizzas Happy Hour — Session Outside

Sponsored by: Northrop Grumman

Session Chair: Erica Folk, Northrop Grumman

IN-PERSON ONLY – NO STREAMING
FLAMINGO LAWN (Outside – weather permitting)

<table>
<thead>
<tr>
<th>Session Title</th>
<th>Presenter</th>
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<tbody>
<tr>
<td>A Novel Design of High-Temperature Lead-Free Solders for Die-Attachment in Power Discrete Applications</td>
<td>Hongwen Zhang, Indium Corporation (Samuel Lytwynec, Huaguang Wang)</td>
</tr>
<tr>
<td>Evolution and applications of fine-feature solder paste printing for heterogeneous integration</td>
<td>Evan Griffith, Indium Corporation (Sze Pei Lim)</td>
</tr>
<tr>
<td>Understanding Photoresist - Electroplating Bath Interactions Using HPLC Methodology</td>
<td>Irene Popova, Ancosys Inc. (Norbert Schroeder, Ramona Dieckmann, Ancosys GMBH; Gerard Gomes, Jeremy Golden, KernLab)</td>
</tr>
<tr>
<td>Electrochemical Express Analysis of Organic Additives in Tin and Tin-Silver Wafer-Level Packaging Plating Baths</td>
<td>Michael Pavlov, ECI Technology (Zhi Liu, Danni Lin, Eugene Shalyt, Isaak Tsimberg)</td>
</tr>
<tr>
<td>Challenges and Novel Approaches for the Development of Hardware-related Trustworthy Electronics</td>
<td>Andreas Middendorf, Fraunhofer Institute for Reliability and Microintegration (Erik Jung)</td>
</tr>
</tbody>
</table>

7:30 PM – 9:00 PM:
President’s Party & Microelectronics Foundation Reception — Outside
SKYVIEW or ARLO PATIO (restaurant - Outside – weather permitting)
In-Person / Live Program Agenda:

**Wednesday, October 13, 2021**

7:00 AM – 8:00 AM: INTERNATIONAL LIAISON COMMITTEE MEETING (INVITE ONLY)
GOLDEN STATE BOARDROOM - Board Room / U
Streaming - Remote speakers & attendees can connect (ZOOM / TEAMS is enough)

7:00 AM - 6:30 PM  Registration Open
IMAPS Registration (T&C Foyer)

11:00 AM - 6:45 PM   Exhibit Hall Open
IMAPS Exhibit Hall (Golden State Ballroom)

7:00 AM - 8:00 AM   Breakfast & Coffee in Foyer
IMAPS Registration (T&C Foyer)

8:00 AM – 9:45 AM: Day 2 Announcements & Keynotes
Room: Town & Country A
Streaming - Remote speakers & attendees can connect

Sponsored by:

**8:00 AM – 9:45 AM: Day 2 Announcements & Keynotes**

**Room:** Town & Country A

**Streaming:** Remote speakers & attendees can connect

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**8:15 AM – 9:00 AM: Keynote 1:**

**Keynote Presentation 3: VIRTUAL PRESENTATION**

**PACKAGING TECHNOLOGIES FOR INTEGRATED PHOTONICS**

Integrated photonics combine multiple optical and electronic functions onto a single semiconductor chip, shrinking footprint and cost significantly. This enables new applications such as faster and more portable communication devices, quantum computing, smart and minimally invasive surgical devices, personal medical diagnostics, food quality monitoring, autonomous vehicles, space-based systems, the internet-of-things and augmented reality systems. There have been significant developments to realize cost-effective photonic chip fabrication processes, but there now exists a manufacturing bottleneck associated with device packaging which is impeding the growth of these emerging markets. This talk will give an overview of existing photonic and electronic packaging technologies and future challenges. The talk will also present how many of these packaging technologies being brought to commercialization through a large-scale Pilot Line funded by the European Commission. Called PIXAPP, the Pilot Line provides users with a wide range of advanced photonic and electronic packaging technologies, with the ability to scale manufacturing to medium volumes. PIXAPP is strongly focused on offering standardized packaging technologies, and is working with its global partners to establish a detailed set of packaging design rules and technology roadmap.

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**Peter O'Brien, Tyndall Institute**

**Head of the Photonics Packaging & Integration Group**

Prof. Peter O'Brien is Director of the European Photonics Packaging Pilot Line (www.pixapp.eu), leads the new European Photonics Academy (www.photonhub.eu) and head of the Photonics Packaging & Integration Group at the Tyndall Institute (www.tyndall.ie) at University College Cork in Ireland. His research group develops packaging and device integration solutions for a wide range of photonic-based applications. The PIXAPP Pilot Line, which he coordinates, is currently engaged with over 140 companies from across the world, developing packaging solutions for applications including communications, quantum computing, medical diagnostics and LIDAR. Prof. O'Brien previously founded and was CEO of a start-up company manufacturing specialty photonic systems for bio-imaging applications, which he sold in 2009. Prior to this, he was a post-doctoral scholar at the California Institute of Technology and a research scientist at NASA's Jet Propulsion Laboratory, where he was involved in the development of submillimetre wave devices for remote sensing applications. He received his degree and PhD in Physics from Trinity College Dublin and University College Cork respectively.
HIGH RELIABILITY MICROELECTRONIC PACKAGING

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For several decades, microelectronic industries and relevant Academic communities have invested tremendous effort in developing electronics to introduce many breakthroughs and revolutions in packaging technologies and repetitive efforts to address traditional problems. In recent years, slowdown in Moore’s law scaling and the challenging economics associated with adopting new Silicon nodes has led to an industry emphasis on chiplet-based architectures that require advanced packaging options ranging from MCM to CoWoS® for HPC, Networking, Cloud Services, Emulation and other applications.

Advanced heterogeneous packaging based on 2.5D CoWoS®/3D/Fan-out/Optical or other platforms are required to address various Logic and memory integration. The inexorable push towards higher performance “system in a package” solutions coupled with silicon technology scaling and cost challenges is expected to stretch the heterogeneous packaging boundaries much further. Thermal solution is also becoming an active area of focus as the power levels are expected to push well beyond 500W.

In the presentation we will examine latest Heterogeneous Packaging industry trends with some FPGA examples, challenges and considerations from a product perspective. Industry roadmap projections do not adequately tackle questions on optimal package configurations that maximize silicon performance while addressing manufacturability, reliability and thermal constraints. Especially, heterogeneous integration of chiplet or stacked dies in a single package, leads to ever-increasing localization of heat and thermo-mechanical reliability challenges with the package and board integration. This presentation will also touch upon some of trends and challenges in these areas and interplay with the package.

Suresh Ramalingam, Xilinx Fellow

Dr. Suresh Ramalingam graduated in 1994 with a Ph.D. in Chemical Engineering from Massachusetts Institute of Technology, Cambridge. He holds 40 US Patents, 30+ publications, 2013 SEMI Award, Ross Freeman Award for Technical Innovation, ECTC 2011 Conference Best Paper Award, IMAPS 2013 and 2014 Conference Best Paper Awards for 2.5D/3D and contributed a book chapter on 3D Integration in VLSI Circuits. He started his career at Intel developing Organic Flip Chip Technology for Microprocessors which was implemented on Pentium II (Intel’s first flip chip product) in 1997. The effort received personal recognition from then CEO Craig Barrett. As one of the co-founders and Director of Packaging Materials at Scion Photonics started in 2000, he helped develop DWDM modules used by major communication companies. JDS Uniphase acquired Scion Photonics in 2002. After joining Xilinx in 2004, he has experienced various roles from Substrate Technology & Sourcing, Design Management to Packaging Technology Development. As a Xilinx Fellow, he currently manages Advanced Packaging Interconnect Technology Development including TSV/3D/Optical for Xilinx FPGA products. Thermal and Mechanical Enablement at Board/System Level is a key focus area to push the power/performance envelope and this is an area he currently manages for Xilinx Alveo and SOM products.
## Wednesday Morning Technical Sessions

**10:15 AM – 11:40 AM:**

<table>
<thead>
<tr>
<th>Time</th>
<th>TRACK 1</th>
<th>TRACK 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>10:15 AM-</td>
<td><strong>Wafer Level Session 2:</strong> WAFER / HYBRID BONDING</td>
<td><strong>Wafer Level Session 3:</strong> WLCSP (FAN IN AND ADVANCE MATERIAL)</td>
</tr>
<tr>
<td>5:40 PM</td>
<td>Session Chairs: Konstantin Yamnitskiy, Medtronic</td>
<td>Session Chairs: Rey Alvarado, Qualcomm</td>
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<tr>
<td></td>
<td>Erica Folk, Northrop Grumman Corp.</td>
<td>SooSan Park, JCET Group</td>
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<td>IN-PERSON Room: Town &amp; Country A</td>
<td>IN-PERSON Room: Town &amp; Country B</td>
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<tr>
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<td>No Streaming – All in-person</td>
<td>No Streaming – All in-person</td>
</tr>
<tr>
<td>10:15 AM-</td>
<td>**State-of-the-Art and Outlooks of Chiplets Heterogeneous Integration</td>
<td>**High-Accuracy Pick-and-Place of Multiple Dies in Parallel Enabled</td>
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<tr>
<td>10:40 AM</td>
<td>and Hybrid Bonding**</td>
<td>by Self-Alignment**</td>
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<tr>
<td></td>
<td>John Lau, Unimicron Technology Corp.</td>
<td>Chris Scanlan, Besi Austria GmbH (Birgit. Brandstätter, Benedikt Auer,</td>
</tr>
<tr>
<td></td>
<td>**Prevention of Thinned Wafer Deformation During Thermocompression</td>
<td>Besi Austria GmbH; Sabine Scherbaum, Fraunhofer EMFT)</td>
</tr>
<tr>
<td></td>
<td>Bonding Supported by Temporary Bonding Materials**</td>
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<tr>
<td></td>
<td>Alice Guerrero, Brewer Science, Inc. (Pieter Bex, Alain Phommahaxay,</td>
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<td></td>
<td>Eric Beyne, IMEC; Andy Jones, Daqjie Dong, Brewer Science, Inc.;</td>
<td></td>
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<td></td>
<td>Arthur Southard, Brewer Science Taiwan)</td>
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<tr>
<td>11:15 AM-</td>
<td><strong>Photonic Debonding for Wafer-Level Packaging</strong></td>
<td><strong>Advanced Protected Fan-In WLCSP</strong></td>
</tr>
<tr>
<td>11:40 AM</td>
<td>Vikram Turkani, NovaCentrix (Vahid Akhavan, Kurt Schroder, NovaCentrix;</td>
<td>Douglas Hackler, American Semiconductor, Inc. (Ed Prack, MASIPLLC)</td>
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<td></td>
<td>Xiao Liu, Luke Prenger, Xavier Martinez, Brewer Science)</td>
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</tbody>
</table>

### Networking & Lunch in Exhibit Hall

**11:45AM – 1:30 PM:**

**Networking & Lunch in Exhibit Hall**

IMAPS Exhibit Hall (Golden State Ballroom)

**Sponsored by:**

![MRSI](image-url)
**1:30 PM – 5:45 PM: Wednesday Afternoon Technical Sessions**

<table>
<thead>
<tr>
<th>TRACK 1</th>
<th>TRACK 2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1:30 PM-3:25 PM</strong></td>
<td><strong>Materials Session 2:</strong> ADVANCED INTERCONNECTS / WIRE BOND</td>
</tr>
<tr>
<td>Advanced Packaging Session 2: INVITED SESSION: OPTICAL CO-PACKAGING <strong>Hybrid Session</strong></td>
<td>Session Chairs: Dan Krueger, Honeywell Jim Will, SkyWater Technology</td>
</tr>
<tr>
<td>Session Chairs: Tolga Tekin, Fraunhofer IZM <em>VIRTUAL</em></td>
<td>IN-PERSON</td>
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<tr>
<td>HYBRID SESSION</td>
<td>Room: Town &amp; Country B No Streaming – All in-person</td>
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<td>Room: Town &amp; Country A Streaming - Remote speakers &amp; attendees can connect</td>
<td></td>
</tr>
<tr>
<td><strong>1:30 PM-1:55 PM</strong></td>
<td><strong>JEDEC’s Generation of Wire Bond Pull Test Methods to Address Pulling of Copper Wire Bonds</strong></td>
</tr>
<tr>
<td>Detachable Fiber Assembly for Co-packaged Optics Hesham Taha, Teramount Ltd.</td>
<td>Curtis Grosskopf, IBM Corporation</td>
</tr>
<tr>
<td><strong>2:00 PM-2:25 PM</strong></td>
<td><strong>Optical Interconnect in Co-Packaged Optics System</strong></td>
</tr>
<tr>
<td>Tiger Ninnomiya, SENKO Advanced Components, Inc.</td>
<td>Henri Seppänen, Kulicke &amp; Soffa Industries (Siang Tat Chua)</td>
</tr>
<tr>
<td><strong>2:30 PM-2:55 PM</strong></td>
<td><strong>Optimization Of Al Heavy Wire Bonds In WBG Power Module Design For Studying Current Limits And Cross-Talk Reduction</strong></td>
</tr>
<tr>
<td>Mark Wade, Ayar Labs</td>
<td>Utkarsh Mehrotra, NCSU PREES</td>
</tr>
<tr>
<td><strong>3:00 PM-3:25 PM</strong></td>
<td><strong>Advanced Packaging Technology for Novel 1-dimensional and 2-dimensional VCSEL Arrays</strong></td>
</tr>
<tr>
<td>Katarzyna Ławniczuk, Bright Photonics B.V.</td>
<td>Rainer Dohle, Micro Systems Engineering GmbH (Gerold Henning, Maximilian Wallrodt, Micro Systems Engineering GmbH; Christoph Gréus, Christian Neumeyer, VERTILAS GmbH)</td>
</tr>
<tr>
<td><strong>3:25 PM-4:15 PM</strong></td>
<td><strong>BREAK IN EXHIBIT HALL</strong></td>
</tr>
<tr>
<td>IMAPS Exhibit Hall (Golden State Ballroom)</td>
<td>**Continued… INVITED SESSION: OPTICAL CO-PACKAGING <strong>HYBRID SESSION</strong></td>
</tr>
<tr>
<td><strong>4:15 PM-5:45 PM</strong></td>
<td><strong>Wafer Level Session 4: PANEL-LEVEL FAN OUT</strong></td>
</tr>
<tr>
<td>Continued… INVITED SESSION: OPTICAL CO-PACKAGING <strong>HYBRID SESSION</strong></td>
<td>Session Chairs: Li-San Chan, Heraeus Vivek Dutta, Adveniente LLC</td>
</tr>
<tr>
<td><strong>4:30 PM-4:40 PM</strong></td>
<td>IN-PERSON</td>
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<tr>
<td>Marika Immonen, TTM Technologies Inc.</td>
<td>Room: Town &amp; Country B No Streaming – All in-person</td>
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<tr>
<td><strong>4:45 PM-5:10 PM</strong></td>
<td><strong>Lithography Solutions for Submicron Panel-Level Packaging</strong></td>
</tr>
<tr>
<td>Bardia Pezeshki, AvicennaTech</td>
<td>Doug Shelton, Canon USA</td>
</tr>
<tr>
<td><strong>5:15 PM-5:45 PM</strong></td>
<td><strong>Adaptive Patterning Methods and Applications</strong></td>
</tr>
</tbody>
</table>
5:45 PM – 6:45 PM: Happy Hour in Exhibits  
IMAPS Exhibit Hall (Golden State Ballroom)  
Sponsored by:

![ASE GROUP](image)

6:45 PM – 8:30 PM: EVENING KEYNOTE & PANEL SESSION  
HYBRID - Room: Town & Country A  
Streaming - Remote speakers (1 keynote then panel discussion) & attendees can connect  
Sponsored by:

![MATERION](image)

EVENING KEYNOTE  
Introduced by Panel Moderator – Jan Vardaman...  
6:45 PM – 7:20 PM: Evening Keynote  

**Evening Keynote Presentation:** VIRTUAL PRESENTATION  
**CHALLENGES AND OPPORTUNITIES OF PACKAGING FAB NEAR THE END OF MOORE’S ERA**

While the semiconductor industry has relied on CMOS scaling for decades, heterogeneous integration of a diverse set of technologies is now an important way to drive optimum power-performance-area-cost (PPAC) and turn-around-time (TAT) beyond what was possible with monolithic integration only. Various chiplet packaging solutions, such as 2D, 2.5D, 3D and 3.5D are necessary to develop fine pitch interconnection evolutions with the Cu hybrid bonding or fine pitch microbump interconnection.

In this presentation, package FAB solutions are to be introduced and discussed in terms of challenges and opportunities for emerging high-end computing and mobile processor platforms. In addition, Fanout WLP, RDL interposer, high-performance 3D SIP and Integrated Stacked Capacitor (ISC) are introduced.

Seungwook “Stewart” Yoon, Samsung Electronics  
Corporate VP / Package Technology Planning, Test & System Package

Dr. YOON is currently working as Corporate VP/Head of Team of Package Technology Planning, Test & System Package, Samsung Electronics. Prior to joining Samsung, He was director of group technology strategy, STATS ChipPAC. He also worked deputy lab director of MMC (Microsystem, Module and Components) lab, IME (Institute of Microelectronics), A*STAR, Singapore. “YOON” received Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds MBA degree from Nanyang Business School, Singapore. He has over 300 journal papers, conference papers and trade journal papers, and over 20 US patents on microelectronic materials and electronic packaging. Served as technical committee member of various international packaging technology conferences, EPTC, ESTC, IMAPS, IWLPC and SEMI.

Panel Session moderated by Jan Vardaman...  
7:20 PM – 8:30 PM:

**PANEL SESSION: NEXT GENERATION PACKAGES: ARE WE READY?**

**Moderator:** Jan Vardaman, President and Founder of TechSearch International, Inc.

New package options are required to meet the needs of advanced silicon nodes and cost reduction. Adoption of Co-packaged optics is anticipated. The industry requires a health infrastructure to meet future packaging needs including heterogeneous integration and chiplets. Are we ready? What infrastructure issues need to be addressed? This panel discusses challenges in meeting the needs of next generation packaging and provides insight into potential solutions.

**PANELISTS:**

Ravi Agarwal, Facebook - Technical Sourcing Manager  
Tom DeBonis, Intel – Engineering TD Manager, Assembly/Test Technology Development  
Suresh Ramalingam, Xilinx - Fellow  
Ashkan Seyedi, Nvidia – Silicon Photonics Product Architect  
Raja Swaminathan, AMD – Senior Fellow and Advanced Packaging Leader  
Seungwook “Stewart” Yoon, Samsung Electronics - R&D Strategy, Corporate VP/Head of Team

Includes Beer, Wine and Appetizers
In-Person / Live Program Agenda:
Thursday, October 14, 2021

7:00 AM - 3:00 PM  
Registration Open
IMAPS Registration (T&C Foyer)

7:00 AM - 8:00 AM  
Breakfast & Coffee in Foyer
IMAPS Registration (T&C Foyer)

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8:00 AM – 9:45 AM:   Day 3 Announcements & Keynotes
Room: Town & Country A
Streaming - Remote speakers & attendees can connect

Sponsored by:

Introduced by General Chair-elect 2022...
8:15 AM – 9:00 AM: Keynote 1:

Keynote Presentation 5:  VIRTUAL PRESENTATION
ADVANCED PACKAGING IS THE FUTURE OF SEMICONDUCTOR INDUSTRY!

Although Moore’s Law has remained alive for over five decades, it is no longer cost-efficient. When it comes to advanced lithographic nodes, lesser manufacturers can keep up. Now there are only three leading-edge players, Intel, Samsung and TSMC. The industry is now diligently using advanced packaging technologies to put multiple advanced and/or mature chips in a single package. Together with 3D packaging this extends Moore’s Law at system-level. Times have changed. The industry is seeking alternatives to design and manufacture the latest Systems on Chips (SoCs) using System in Package (SiP) and chiplet-based approaches by leveraging on Advanced Packaging technology. The total IC packaging market was worth $68B in 2020. Advanced Packaging (AP) was worth $30B and is expected to grow at CAGR2020-2026 of 7.7% to reach $47.5B in 2026. At the same time, traditional packaging market will grow at CAGR2020-2026 of 4.3% and total packaging market will grow at CAGR2020-2026 of 5.9% to $47.9B and $95.4B, respectively. Compared to traditional packaging which will grow at 3.2% CAGR2014-2026, AP will grow more than 2 times quicker, with its CAGR2014-2026 of 7.4%. Two Advanced Packaging roadmaps are foreseen – scaling (going to sub10 nm nodes) and functional (staying above 20nm nodes). Both roadmaps hold more multi-die heterogeneous integration (SiP) and higher levels of package customization in the future. 3 competitive areas are present and will continue to develop – PCB vs. substrate, substrate vs. fan-out, fan-out vs. 2.5D/3D. The main innovations in Advanced Packaging are: decreasing Cu pillar pitch; RDL/substrate development for L/S <10 um (thin film RDL, SAP, Cu damascene RDL and hybrids bonding thereof); further TSV integration (2.5D/3D and MEMS/CIS).

Jean-Christophe Eloy, Yole Développement
President and CEO

Jean-Christophe Eloy is President and CEO of the Yole Développement company. Created in 1998, the market research & strategy consulting company has grown to become a group of companies providing marketing, technology and strategy consulting, media in addition to corporate finance services. His mission is to oversee the strategic direction of Yole Group of Companies.

With System Plus Consulting, Blumorpho, PISEO and Yole Développement, Yole Group of Companies has developed a unique understanding of technologies to accurately evaluate markets, applications, solutions and strategies.

With more than 70 analysts, including PhD and MBA qualified industry veterans, the group collects information, identifies trends, challenges, emerging markets, and competitive environments and then turns that information into results to give a complete picture of the industry’s landscape.

All year long, Jean-Christophe builds deep relationships with leading semiconductor companies, discussing and sharing information across his global network. His aim is to get a comprehensive understanding of their strengths and guide their success.
For glass, it would be inappropriate to speak of a new material in microelectronics. It is considered one of the oldest man-made materials and is also regularly used in electronic packaging already. However, if we look at the fundamental material properties of glass, the only question that really arises is: why isn’t it used in a greater number of applications? The answer to the question lies in the widespread belief that glass is difficult or uneconomical to process on a microscale. This presentation will describe how recent developments in the field of laser-induced deep etching are helping to enable novel packages and bring glass to a new era in micro-electronics.

Roman Ostholt, LPKF Laser & Electronics AG
Managing Director
Roman Ostholt studied mechanical engineering at RWTH Aachen University and graduated in 2007 as Dipl.-Ing. He started his career as a research fellow at the Fraunhofer Institute of Laser Technology. After finishing his doctoral thesis in 2011, he joined LPKF Laser & Electronics AG as an Innovation Manager. In 2014 Roman Ostholt became Vice President Technology Management of LPKF and in that role, he was responsible for the development of LIDE technology. He is inventor and co-inventor of multiple patents in that field. Based on these developments, he has been driving the establishment and expansion of a new business field for glass micromaching from 2018. Since 2020 he is in charge of the whole Business Unit “Electronics” at LPKF Laser & Electronics AG.
## Thursday Morning Technical Sessions

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<tr>
<td>10:15 AM - 12:10 AM</td>
<td><strong>Optimization Session 1:</strong> MANUFACTURING / PROCESS OPTIMIZATION</td>
<td><strong>Materials Session 3:</strong> PLATING, COATING &amp; CONTAMINATION</td>
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<td></td>
<td>Session Chairs: Dongshun Bai, Brewer Science</td>
<td>Session Chairs: Doug Shelton, Canon USA</td>
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<td>Lyndon Larson, DuPont Electronics</td>
<td>Douglas C Hopkins, North Carolina State University</td>
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<td>No Streaming – All in-person</td>
<td>No Streaming – All in-person</td>
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<tr>
<td>10:15 AM - 12:10 PM</td>
<td>Eliminate Costly Component Out Of Pocket Defect Condition during Semiconductor IC Transport/Handling</td>
<td>Comprehensive Characterization of Inorganic/Organic Components in Neutral Tin Plating Bath for Electronics Applications</td>
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<td></td>
<td>Craig Blanchette, BAE Systems</td>
<td>Eugene Shalyt, ECI Technology (Jingjing Wang, Vishal Parekh, Chuanan Bai, Guang Liang)</td>
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<td>Darby Davis, Gel-Pak; Jennifer Nunes, Delphon</td>
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<tr>
<td>10:45 AM - 11:10 AM</td>
<td>Wire Sway/Sweep Detection in Wire-bonded Advanced Package Assemblies Using In-line High Resolution Automated X-ray Inspection (HR-AXI) in High Volume Manufacturing</td>
<td>Characterization of formaldehyde-free electro-less copper plating solution for SAP</td>
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<tr>
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<td>Nabil Dawahre, SVXR (Silicon Valley X-ray)</td>
<td>April Laborite, Uyemura USA (Masaharu Takeuchi)</td>
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<tr>
<td>11:15 AM - 11:40 AM</td>
<td>Enhanced UVA LED-Cured Conformal Coatings for Printed Circuit Boards</td>
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<td>Neal Pfeiffenberger, Sartomer (Saeid Biria)</td>
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<tr>
<td>11:45 AM - 12:10 PM</td>
<td>Contamination Troubleshooting for Microelectronics Packaging</td>
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<td>Victor Chia, Air Liquide Electronics - Balazs NanoAnalysis</td>
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### Special Invited Session: HETEROGENOUS INTEGRATION ROADMAP

**Heterogenous Integration Roadmap** (LIVE – VIRTUAL all remote)

**Session Chair:** Bill Chen, ASE

<table>
<thead>
<tr>
<th>Time</th>
<th>Topic</th>
<th>Speaker(s)</th>
</tr>
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<td>12:15 pm – 12:40 pm</td>
<td>Overview</td>
<td>Bill Bottoms / Bill Chen</td>
</tr>
<tr>
<td>12:40 pm – 1:05 pm</td>
<td>Medical Health &amp; Wearable</td>
<td>Mark Poliks</td>
</tr>
<tr>
<td>1:05 pm – 1:30 pm</td>
<td>MEMS &amp; Sensor Integration</td>
<td>Shafi Saiyid &amp; MaryAnn Maher</td>
</tr>
<tr>
<td>1:30 pm – 1:45 pm</td>
<td>Break</td>
<td>Tom Salmon</td>
</tr>
<tr>
<td>1:45 pm – 2:10 pm</td>
<td>Supply Chain</td>
<td>Sohrab Attabajhani</td>
</tr>
<tr>
<td>2:10 pm – 2:35 pm</td>
<td>Security</td>
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<tr>
<td>2:35 pm – 3:00 pm</td>
<td>Round Table Discussion + Q&amp;A from Chat</td>
<td></td>
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</table>

**3:00 PM:** CLOSING REMARKS at Conclusion of HIR Session

**General Chair/elect**
Thursday, October 14, 2021...

continued

3:00 PM – 4:00 PM:
CHAPTER LEADERSHIP MEETING
GOLDEN STATE BOARDROOM
Board Room / U
Streaming - Remote speakers & attendees can connect
(ZOOM / TEAMS is enough)
On-Demand Presentations:

**A - Manufacturing Optimization**
Track Chairs: Dongshun Bai, Brewer Science
Suresh Jayaraman, Amkor

**B - Wafer Level/Panel Level (Advanced RDL)**
Track Chairs: Tarak Railkar, Qorvo
Rey Alvarado, Qualcomm

**C - High Performance-High Reliability**
Track Chairs: Erica Folk, Northrop Grumman
Ivan Ndip, Fraunhofer IZM

**D - Advanced Packaging (Flip Chip/2.5D/3D/Optical)**
Track Chairs: Frank Eberle, Northrop Grumman Corp.
Jaimal Williamson, TI

**E - Advanced Process & Materials (Enabling Technologies)**
Track Chairs: Benson Chan, Binghamton Univ.
Mark Hoffmeyer, IBM

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**TPM1 - Design, Modeling & System Simulation**
Session Chairs: Lei Fu, AMD
ML/AI in Semiconductor Packaging & Electronics Manufacturing
Dongkai Shangguan, Adapdix

Automatic Design Rule Derivation for Assembly Design Kits (ADK)
Andy Heinig, Fraunhofer IIS/EAS

Design Constraints and Scale Down Evolution in Advanced Semiconductor Packages
Byong Jin Kim, Amkor Technology Korea, Inc.
(Sang-Hyeon Lee, JaeBeom Shim, JinYoung Khim, Amkor Technology Korea, Inc.; Nam-Hee Cho, Inha University)

**TPM2 - Wafer-level Fan out & Advanced RDL**
Session Chairs: Frank Wei, Disco
Wen Yin, Qualcomm

High UV Transmission Glass Carriers for Advanced Packaging
Jai Zhang, Corning Incorporated

Latest Technology of Wafer Coating Material for Advanced Packages
Ryuji Hiroswa, Sumitomo Bakelite Co., Ltd.

Numerical Simulation on the Warpage of Reconstructed Wafer During Encapsulation Process
HU Zhen, JCET Advanced Packaging Co. Ltd.

Proven Methodologies to Meet FOWLP Manufacturing Process Requirements for Metal Filled Areas and Plans
Kendall Hiles, Siemens EDA

**TPM3 - RF Packaging & Design**

Stabilized Sanathanan-Koerner Iteration for Rational Transfer Function Approximation of Scattering Parameters
Arif Engin, San Diego State University (Jose Tomimatzu, Andrew Ma, Daniel Deaton)

Design and Implementation of Harmonic RFID Based on Conventional UHF System
Aditya Purandare, Michigan State University (YiHang Chu, Deepak Kumar, SaiKat Mondal, Prem Chahal)

**TPM4 - Flip Chip**
Warpage Simulation Study by Trace Mapping Method for FCCSP with ETS Substrate
Yun-Ming Zhang, SPIL

Effect of Solder Alloy, and Package Construction on Board Level Reliability of a Flip-chip Package
Sudan Ahmed, NXP semiconductor Inc. (Mollie Benson, Nishant Lakhera, Andrew Mawer)

**TPM5 - Advanced Substrate Materials**
Session Chairs: Sylvain Pharand, IBM
Aric Shorey, Mosaic Microsystems

Cu Crystal Structures in Plated Microvias. Recrystallisation & a Means to Identify Joints at Risk of Premature Failure
Roger Massey, Atotech Deutschland GmbH (Tobias Bernhard, Killian Klaeden, Sebastian Sarwell, Stefan Kempa, Edith Steinheuser, Frank Bruning)

Emergence of glass solutions for 5G and Heterogeneous Integration
Shelby Nelson, Mosaic Microsystems (Aric Shorey, David Levy, Paul Ballentine)

Verification of Compartmental Electromagnetic Interference Shielding Effect with imprint-Through Mold Via (i-TMV) for RF
Motohiro Negishi, Showa Denko Materials Co., Ltd. (Tomoaki Shibata, Xinxiong Li, Naoya Suzuki)

Pre-applied Sinter Paste with Advanced Die Interconnect Technology
Habib Mustain, Heraeus Electronics

Low Transmission Loss Cu Wirings with Smooth Seed Layer and High Adhesion against Dielectrics
Kazue Hirano, Showa Denko Materials Co., Ltd.
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**WPM1 - Advanced Materials, Packaging, Reliability**
- Session Chairs: Varughese Mathew, NXP Semiconductors
- Galvanic Corrosion Behavior of Ag filled Electrically Conductive Adhesive on Sn plated of Surface Mount Chip Resistor
  - Onanong Phosie, NXP Semiconductors, Inc. (Chayathorn Saklang, Amar Mavinkurve, Kornteenee Pairpisit, Kittichai Fakpan)

**MAXQFP: NXP’s New Package Solution for Automotive Application**
- Chu-Chung (Stephen) Lee, NXP Semiconductor, Inc. (XS Pang, JZ Yao, TuAnh Tran, Andrew Mawer)

**WPM2 - WLCSP (Fan In and Advance Material)**
- Low Temperature Curable Low Dk & Df Polyimide for Antenna in Package
  - Hitoshi Araki, Toray (Akira Shimada, Hisashi Ogasawara, Masaya Jukeli, Masao Tomikawa)

**Effect of Novel SAC-Bi Solder Joints on Electromigration Reliability for Wafer Level Chip Scale Packages**
- Min-Yan (Brian) Tsai, Advanced Semiconductor Engineering (ASE) (Yung-Sheng Lin, Chin-Li Kao, Shan-Bo Wang, Ting-Chun Lin, Yun-Ching Hung)

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**WPM4 - INVITED SESSION: Optical Co-Packaging**
- Session Chairs: Tolga Tekin, Fraunhofer IZM Karl Friedrich Becker, Fraunhofer IZM

**WPM5 - Advance Interconnects - Wire Bond**
- Stefan Schmitz, Bond-IQ GmbH
  - Advanced Bonding Interface Inspection Technique for Process Optimization in Heavy Wire Bonding
  - Stefan Schmitz, Bond-IQ GmbH (Martin Schneider-Ramelow, Fraunhofer IZM)
  - Advanced Wire Bonding Standards for European Automotive and Power Electronics Industry
  - Stefan Schmitz, Bond-IQ GmbH (Martin Schneider-Ramelow, Fraunhofer IZM)
  - 645b Experimental Parameter Identification and Validation of a Process Model for Ultrasonic Heavy Wire Bonding
  - Reinhard Schmemmel, Paderborn University (Ludger Klahold, Nico Müller, Tobias Hemsel, Walter Sextro)
### On-Demand Presentations:

**A - Manufacturing Optimization**
- Track Chairs: Dongshun Bai, Brewer Science
  - Suresh Jayaraman, Amkor

**B - Wafer Level/Panel Level (Advanced RDL)**
- Track Chairs: Tarak Railkar, Qorvo
  - Rey Alvarado, Qualcomm

**C - High Performance-High Reliability**
- Track Chairs: Erica Folk, Northrop Grumman
  - Ivan Ndip, Fraunhofer IZM

**D - Advanced Packaging (Flip Chip/2.5D/3D/Optical)**
- Track Chairs: Frank Eberle, Northrop Grumman Corp.
  - Jaimal Williamson, TI

**E - Advanced Process & Materials (Enabling Technologies)**
- Track Chairs: Benson Chan, Binghamton Univ.
  - Mark Hoffmeyer, IBM

**THAM1 - Process Optimization**
- Session Chairs: Santosh Kudtarkar, Analog Devices
  - Bora Baloglu, Amkor Technology

**Implementing of Trusted Manufacturing & AI-based Process Optimization into Microelectronic Manufacturing**
- Karl-Friedrich Becker, Fraunhofer IZM
  - Steve Voges, Fraunhofer IZM
  - Peter Freuhauf, Matthias Heimann, Siemens AG
  - Andreas Hofmeister, Stefan Gottwald, Sensorik Bayern
  - Salar Mehrafsun, Wagenbrett GmbH

**Coronavirus, Chip Boom, and Supply Shortage: The New Normal for Global Semiconductor Manufacturing**
- Stephen Rothrock, ATREG, Inc.

**Burn-in Testing (BIT): To BIT or Not to BIT, That's The Question**
- Ephraim Suhir, ERS Co.

**THAM2 - Module Warpage / Plating Solution Contamination Mitigation**
- Session Chairs: Tie Wang, Qualcomm

**The Pivotal Role of Uniformity of Electrolytic Deposition Processes to Improve the Reliability of Advanced Packaging**
- Ralf Schmidt, Atotech

**THAM3 - High Reliability Packaging**
- **Fine-pitch Copper Pillar Flip Chips in High Reliability Applications**
  - Catherine Farrum, Northrop Grumman Corp. (Kaysar Rahim)

**Additively Manufactured Extreme Temperature Electronics Packaging**
- David Shaddock, General Electric Global Research

**THAM4 – Interconnect**
- **High Density Package Design Platform and Assembly Design Kit**
  - Chih-Yi Huang, Advanced Semiconductor Engineering Inc. (ASE)

**Enhancing the Paste Release on 55µm pads with Water-Soluble Type 7 SAC305 Solder Paste for High Density SIP application**
- Senthil Kumar Balasubramanian, Heraeus Materials Singapore

**Impact of Bonding Sequence on Contact Resistance in Hybrid Bonding of Via-middle TSV Wafer**
- Naoya Watanabe, Advanced Industrial Science and Technology (Hirosi Yamamoto, Takahiko Mitsu, Eiichi Yamamoto, Okamoto Machine Tool Works, Ltd)

**THAM5 - Novel Fabrication Methods**
- **RF and Reliability Characteristics of Printed Interconnects**
  - Kurt Christenson, Optomec (David Sessions, Optomec; Steve Gonya, Joe Jendrisak, Mike Geyer, Mark Halliday, Tom Rovere, Lockheed Martin)

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**POSTER SESSION:**

**Thermal and Reliability Comparison of Double-Sided Cooled Power Modules Using Organic and Ceramic Insulated Substrate**
- Tzu-Hsuan Cheng, NCSU PREES (Douglas Hopkins)

**Epoxy Flux Prevent Hot Tear at VIPPO Solder Joints**
- Ning-Cheng Lee, Consultant (Elaina Zitto, Dave Bedner, Indium Corporation)

**Highly Accelerated Lifetime Testing in Power Electronics**
- Bernhard Czerny, TU Wien (Golta Khatibi)
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www.heraeus-electronics.com

Heraeus Electronics has been a leading materials supplier to the semiconductor industry for many years. Widely known as a technology leader for bonding wires and Thick Film, Heraeus has been tackling the next technological challenge in semiconductor packaging and developing best-in-class advanced packaging solutions. Heraeus offers an excellent solder paste, Welco AP5112 specially developed for ultra-fine pitch applications with best-in-class void performance. Through all-in-one print processing, steps are reduced and SIP assembly processing becomes simplified. With its Welco technology Heraeus offers powder for Type 6, 7 and beyond. In addition to new solder paste developments, Heraeus has developed AgCoat Prime, a gold coated silver wire which offers the highly competitive Memory, LED and Smartcard market a substitute for gold bonding wire. This gold-coated silver bonding wire ensures high performance at a lower cost.

Hesse Mechatronics, Inc.
108
Tustin, CA USA
www.hesse-mechatronics.com

Hesse Mechatronics is an interconnection solutions provider. We make all types of wire bonders (ball, wedge, ribbon) as well as ultrasonic smart welders. Hesse Customer Solutions provides engineering, design, and production services to the microelectronics industry. We also provide all levels of automation.

Hi-Rel Laboratories
507
Spokane, WA USA
www.HRLabs.com

Hi-Rel Laboratories is known throughout the world as a leader in qualifying parts for aerospace and commercial use. Whether you need Destructive Physical Analysis, Materials Analyses, Failure Analysis, NDT, or Upgrading your commercial parts, we can do it.

Honeywell FM&T
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www.kcnsd.doe.gov/careers

Honeywell FM&T manages and operates the U.S. Department of Energy’s Kansas City National Security Campus. This state-of-the-art engineering and manufacturing facility produces a wide array of intricate components to enhance the safety and security of our nation’s defense program. For over the last 70 years, our employees have come together to support the warfighter and keep our nation’s nuclear deterrent safe, secure and reliable, now and always.

Hybond Inc.
604
Excondido, CA USA
www.hybond.com

HYBOND, Inc. designs, manufactures and sells: 1. Wire Bonders: Ball Bonders, Wedge Bonders for wire and ribbon, Single Point TAB or Peg Bonders and a variety of adjustable height heated work stages. 2. Die Bonders: Epoxy Die Bonders, Eutectic Die Bonders and Pulsed Heat Systems. 3. DFS Universal Wire Bonder Test Units.

Indium Corporation
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Indium Corporation is a premier materials manufacturer and supplier to the global electronics, semiconductor, thin-film, and thermal management markets. Products include solders and fluxes; brazes; thermal interface materials; sputtering targets; indium, gallium, germanium, and tin metals and inorganic compounds; and NanoFoil®. Founded in 1934, the company has global technical support and factories located in China, Malaysia, Singapore, South Korea, the United Kingdom, and the USA.
**Integra Technologies, LLC**  
**402**  
Wichita, KS USA  
www.integra-tech.com

Integra Technologies is a global leader in the sourcing, packaging, testing and characterization of highly specialized, mission-critical semiconductor components and related value-added services for high-reliability ("Hi-Rel") applications where dependability and failure-free performance are of paramount importance. Integra provides a span of in-house services and capabilities to support a broad variety of Hi-Rel components throughout the entire value-added life-cycle - from prototyping, through testing, and ultimately to volume production. More specifically, Integra specializes in semiconductor die prep, packaging, assembly, test, reliability qualification, DPA and FA service for high-reliability applications. Find out more at: https://www.integra-tech.com

**JST Manufacturing**  
**618**  
Meridian, ID USA  
www.jstmfg.com

Since its founding in 1982, JST’s mission has been to design and build efficient-and-cost-effective cleaning and processing products for cleanroom applications and to support these products with superior customer service. We strive to “be the best at what we do.” We care about our customers and our products. It is dedication to customer satisfaction with over thirty years of JST design and manufacturing expertise which is the foundation of our business. JST is a full service design and manufacturing company. Capabilities consist of Process Development and Applications Testing, Engineering Design and Drafting, Manufacturing and Final Test. Our product lines include: Wet Processing Equipment, Precision Cleaning, and Cleanroom Accessories & Support Equipment.

JST’s manufacturing expertise includes both plastics and metal fabrication as well as mechanical and electrical assembly. We design modular systems that allow easy access to process and maintenance areas. Each and every product is fully tested and packed in our certified 100 Cleanroom. JST’s state-of-the-art facility is headquartered in Boise and encompasses over 60,000 square feet. The latest technology is utilized for cutting and forming the raw materials, whether plastic or metal. Certified welders fabricate the parts which are then leak tested and cleaned prior to mechanical and electrical assembly.

**Kulicke & Soffa Industries**  
**309**  
Fort Washington, PA USA  
www.kns.com

Kulicke & Soffa (NASDAQ: KLIC) is a leading provider of semiconductor and electronic assembly solutions serving the global automotive, consumer, communications, computing and industrial markets. Founded in 1951, K&S prides itself on establishing foundations for technological advancement - creating pioneering interconnect solutions that enable performance improvements, power efficiency, form-factor reductions and assembly excellence of current and next-generation semiconductor devices. Leveraging decades of development proficiency and extensive process technology expertise, Kulicke & Soffa’s expanding portfolio provides equipment solutions, aftermarket products and services supporting a comprehensive set of interconnect technologies including wire bonding, advanced packaging, lithography, and electronics assembly. Dedicated to empowering technological discovery, always, K&S collaborates with customers and technology partners to push the boundaries of possibility, enabling a smarter future.

**Materion Corporation**  
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Mayfield Heights, OH USA  
www.materion.com/advanced-materials

Materion Advanced Materials is an industry leader in providing microelectronic packaging materials for the protection of electronic devices including high-reliability hermetic lids, ceramic packages, preforms, and braze and solder alloys. We offer a comprehensive portfolio of packaging materials in precious or non-precious materials, and we can customize innovative electronic packaging materials to meet your unique needs. In addition to providing high-performance microelectronic packaging materials, Material Advanced Materials a global supplier of premier specialty materials and services for the LED, semiconductor, advanced memory, optical coatings, and large area glass markets. Our offerings include precious and non-precious thin film deposition materials, inorganic chemicals, precision parts cleaning, and precious and valuable metal reclamation. Because of our industry expertise, extensive global manufacturing capabilities, and R&D proficiency, we can meet customers’ material requirements today and are here to partner on future innovations.
Micro Systems Technologies
204, 202
Berlin, Germany
www.mst.com

Micro Systems Technologies (MST) is a leading manufacturer of high-performance electronic components, semiconductor packaging and microelectronics for medical technology, complemented by a wide range of product lifecycle management services. The group develops and produces high-technology solutions for customers around the world, especially for applications in the fields of Life Sciences and Healthcare, Aerospace & Aviation, Internet-of-Things and Sensor technology, as well as Hi-Rel industrial electronics. MST companies are DYCONEX AG in Bassersdorf (Switzerland), Micro Systems Engineering GmbH in Berg (Germany), Micro Systems Engineering, Inc. in Lake Oswego (USA), Litronik in Pirna (Germany) and Micro Connect Technologies in Nuremberg (Germany).

Mini-Systems, Inc.
405
North Attleboro, MA USA
www.mini-systemsinc.com

Mini-Systems, Inc. (MSI) is a world class leader in the manufacture of high-reliability passive components and hermetic packages. For over 50 years MSI has been delivering superior quality products for Military, Aerospace, Communications, Medical and Industrial applications. MSI manufactured products consist of precision: Thin/Thick film Chip Resistors/Networks, QPL Resistors to MIL-PRF-55342, MOS Chip Capacitors, Chip Attenuators, Full Line of RoHS Compliant Products, QPL Jumpers to MIL-PRF-32159/ Mounting Pads, Glass-to-metal seal packages, and Custom Design Packages. Resistors values from 0.1 Ohm to 100GOhm and operating frequencies up to 40 GHz. Absolute tolerances starting at 0.005% and TCRs as low as ±2ppm/°C. Sizes start at 0101. The hermetic packages meet or exceed package evaluation requirements per MI-PRF-38534, Table C-VI. Hermeticity of the packages is less than 10-10 atm cc/ sec per MIL-STD-883, method 1014, condition A4. MSI is ISO 9001 certified. Compliance includes RoHS, REACH, and DFAR. Standard deliveries start in just 2 WEEKS!

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418, 319
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NorCom Systems
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NorCom Systems, Inc. manufactures the NorCom 2020 series Optical Leak Test (OLT) System, which provides automated in-line, full matrix leak testing of hermetically sealed microelectronic, optoelectronic and wafer level devices. The 2020 eliminates the need for helium mass spectroscopy and gross leak bubble testing by utilizing a patented laser interferometer to simultaneously measure gross and fine leaks in hermetic devices. The system provides quantitative leak test results in the industry standard of cc-atm/second helium. The NorCom OLT systems comply with all MIL STD 883 and 750 leak test requirements. The NorCom 2020 is ideal for optoelectronic, semiconductor, MEMS and PCB board mounted devices for military, aerospace, medical, and telecommunication applications.

For more information please contact Chris Aubertin (610) 592-0167

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Palomar Technologies
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We can provide virtually any package you need for prototype and commercial devices, including our exclusive Open-molded Plastic Packages (OmPP®) and Open-cavity Plastic Packages (OCPP®), as well as ceramic and plastic IC packages. Through our substrate development business, we develop turnkey, custom packaging solutions to your specifications to meet your unique packaging requirements.

We perform IC assembly for a variety of package types and materials. Our IC assembly services range from wafer preparation, including backgrinding, dicing, die sort and inspection, to flip chip die bonding, wire bonding, encapsulation, IC package marking/branding, and BGA sphere attach. Through our advanced assembly services, we can accommodate complex packaging structures, including chiplets, flip-chip, stacked die, SiP, MCM, CoB and other structures.

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Anaheim, CA USA
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Senko Advanced Components
206
Marlborough, MA USA
https://www.senko.com/
Senko Advanced Components is a wholly owned subsidiary of the SENKO Group, which is headquartered in Yokkaichi, Japan. From its humble beginnings in 1946, the SENKO Group currently has an estimated annual revenue of $1.4 billion globally. SENKO Advanced Components itself has 14 offices and dozens of design and manufacturing facilities providing local support to customers all around the globe.

SENKO Advanced Components was incorporated in the United States in the early nineties and has since being recognized as one of the industry’s specialists in passive fiber optics interconnect and optical components.
This is due in great part to the design capabilities and high manufacturing capacity in CNC machining, injection molding, and component assembly. To date, SENKO has 46 awarded patents, with more than twenty-five pending.

Sikama International
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www.sikama.com
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Stellar Industries Corp.
603
Millbury, MA USA
www.stellarind.com
Custom manufacturer of metallized ceramic substrates and submounts utilizing direct bond copper(DBC), thin film and thick film. We use AlN, BeO and Alumina as well as other specialty dielectrics. Prototype through high volume production quantities available. Stellar also specializes in manufacturing custom active cooling products such as micro-channel coolers for many industries.

StratEdge Corporation
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Santee, CA USA
www.stratedge.com
StratEdge Corporation, founded in 1992, designs, manufactures, and provides assembly services for a complete line of high-frequency and high-power semiconductor packages operating from DC to 63+ GHz. StratEdge offers post-fired ceramic, low-cost molded ceramic, and ceramic QFN packages, and specializes in packages for extremely demanding gallium arsenide (GaAs) and gallium nitride (GaN) devices. Markets served include telecom, VSAT, broadband wireless, satellite, military, test and measurement, automotive, clean energy, and down-hole. All packages are lead-free and most meet RoHS and WEEE standards. StratEdge assembly services have a Class 1000 cleanroom with Class 100 work areas for performing sensitive operations. It is fully equipped with the most modern assembly equipment, enabling high-speed, deep access, fine wire wedge and ribbon bonding. The component placement die attach system is the fastest and most reliable multiple die-type bonder on the market. It enables StratEdge to offer highly accurate, repeatable placement and includes a station for automated eutectic die attach utilizing proprietary processes that yield ultra-thin, low void solder joints. StratEdge has a variety of lids and options for their attachment and offers post assembly services. StratEdge is an ISO 9001:2015 certified and ITAR registered facility located in Santee, California, near San Diego.

SUSS MicroTec
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Corona, CA USA
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Phoenix, AZ  USA
www.teikoku-taping.com
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www.bakerhughes.com
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We lead the industry in SiP technology advancements.

Amkor was the first OSAT to offer DSMBGA (double sided molded ball grid array) packages as an innovative solution for RF front-end modules used in smartphones and other 5G-enabled devices.

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