11th Annual

International Wafer-Level Packaging Conference & Exhibition

November 11-13, 2014 **DoubleTree Hotel, San Jose, CA**

Conference and Exhibits: November 11-12 **Tutorials:** November 13

SMTA Surface Mount Technology Association

Chip Scale Review

www.iwlpc.com

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Parking for IWLPC attendees is $8/day
Ticket validation ticket located by registration.

Greetings,

On behalf of the *SMTA* and *Chip Scale Review*, we would like to take this opportunity to welcome you to the *11th Annual of the International Wafer-Level Packaging Conference (IWLPC).*

We hope that you will gain knowledge that will be beneficial to both you and your company. We are looking forward to a great conference and exhibition!

Please take a moment to review this show directory. Conference information is featured first; including daily schedules. Next, you will find information on the exhibition, including a complete alphabetical company listing, sponsors, and details on upcoming SMTA events!

A special thank you goes out to our 2014 IWLPC sponsors:

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Enjoy your time at IWLPC. If you have any questions, please visit us at the registration counter or stop by the *Chip Scale Review* booth.

Warm regards,

Patti Coles

Kim Newman

Patti Coles
SMTA - Director of Education

Kim Newman
Chip Scale Review – Publisher

Mark your calendars for IWLPC's 12th Annual Conference October 13-15, 2015
DoubleTree Hotel, San Jose, CA

Sessions at a Glance: Tuesday, November 11th

7:50 AM	**Opening Comments** Keith Cooper, SET North America, Conference General Chair **Oak Ballroom (2nd Floor)**		
8:00 AM	**Keynote Address: Living Connected Through Trillions Sensors** Janusz Bryzek, Ph.D., Chair of the TSensors Summit **Oak Ballroom (2nd Floor)**		
9:00 AM	**Coffee Break** **Exhibit Hall**		
	WLP TRACK | MONTEREY ROOM	**3D TRACK | SAN CARLOS ROOM**	**MEMS TRACK | SANTA CLARA**
	Session 1 – Wafer-Level Final Test & Simulation Chair: Janet Love, Blair-Gordon Associates Co-Chair: Rey Alvarado, Qualcomm	**Session 2 – Temporary Wafer Bonding Integration and Underfill** Chair: Peter Ramm, Ph.D., Fraunhofer EMFT Co-Chair: Ted Tessier, FlipChip International	**Session 3 – 3D MEMS Interconnects and Bonding** Chair: Roger Grace, Roger Grace Associates Co-Chair: Russell Shumway, Amkor Technology
9:45 AM	**Mobile Applications to Enhance Manufacturing Productivity in Advanced Packaging** Shekar Krishnaswamy, Applied Materials, Inc. and Didier Chavet, SanDisk	**Temporary Bonding on the Move Towards High Volume: A Status Update On Cost Of Ownership** Thomas Uhrmann, EV Group	**NCP Versus NCF for Thermocompression MEMS Bonding Using Gold Stud Bumps** Maaike M. Visser Taklo, SINTEF
10:15 AM	**OEE and Production Yield Improvements on WLCSP Devices: Case Study Using Novel Probe Design** Ranauld Perez, Johnstech International	**Addressing Critical Assembly Challenges in 2.5D and 3D IC Assembly** Guilian Gao, Invensas Corporation	**Ceramic Wafer Bonding for Vertically Integrated MEMS** Dirk Wuensch, Chemnitz, University of Technology
10:45 AM	**Material Selection and Its Impact on Coplanarity of Spring Pin Probe Heads** Jiachun Zhou, Smiths Connectors – ID	**Non-Conductive Film (NCF) Underfill for Flip Chip Assembly and High Reliability** Anupam Choubey, The Dow Chemical Company	**A New Manufacturing Approach for Fabricating Next Generation 3-D Interconnects for MEMS and ICs Using Directed Nanoparticle Assembly** Cihan Yilmaz, Northeastern University
11:15 AM	**BVA™ Technology Enabling the Next Generation of Ultra-Fine Pitch Wide-IO Package-on-Package** Rajesh Katkar, Invensas Corporation	**Room Temperature Temporary Bonding/ Debonding Processes for 2.5/ 3D Integration** Tim McCrone, SUSS MicroTec	**3D MEMS Wafer Level Packaging Exemplified by RF Characterized TSVs & TGVs and Integration of Bonding Processes** Peter Ågren, Ph.D., Silex Microsystems AB
11:45 AM	**Lunch Break – Sponsored By Johnstech International** **Bayshore Foyer**		
1:15 PM	**3D PANEL DISCUSSION - HOSTED BY 3D INCITES, INC.** **OAK BALLROOM (2ND FLOOR)**		
	System Level Advantages of 3D Integration **Moderator:** Francoise von Trapp, 3D InCites, Inc. **Panelists:** Rama Alapati, Global Foundries, E. Jan Vardaman, TechSearch International Inc, Mike Gianfagna, eSilicon, Bel Haba, Google Simon McElrea, Energous Corporation		
2:45 PM	**Refreshment Break – Sponsored by Axus Technology** **Exhibit Hall**		
	WLP TRACK | MONTEREY ROOM	**3D TRACK | SAN CARLOS ROOM**	**MEMS TRACK | SANTA CLARA**
	Session 4 - Wafer-Level Materials Chair: Luu Nguyen, Ph.D., Texas Instruments Co-Chair: Boyd Rogers, Ph.D., Deca Technologies	**Session 5 – Bonding and Metrology** Chair: Sumant Sood, KLA-Tencor Co-Chair: Keith Cooper, SET Corporation	**Session 6 - MEMS Wafer Level Packaging** Chair: Maaike M. Visser Taklo, Ph.D., SINTEF Co-Chair: Russell Shumway, Amkor Technology
3:30 PM	**Enhancing WLBGA Board Level Reliability Through SACQ™, A New Lead-Free Solder Material** Tak Sang Yeung, Broadcom Corporation	**Characterization of Stress and Topology In WLP Processes Using CGS Interferometry** David Owen, Ph.D., Ultratech, Inc.	**MEMS WLP Processes and Examples** Micheal Shillinger, Innovative Micro Technology (IMT)
4:00 PM	**Wafer-Level Chip-Scale Packaging for Power Device Operating at High Temperature** Chenping Jia, CTR AG	**Electrostatic Supported Thin-Wafer Processing in 3DIC By Means of the T-ESC Technology** Suresh Biligiri, ProTec Carrier Systems	**The Optimization of MEMS Through The Development of Generic Manufacturing Platforms** Andre Rouzaud, CEA LETI
4:30 PM	**Reconstituted Big-Chip LEDs on Multi-layer Interconnects for High-Brightness Lighting** Liang Wang, Invensas Corporation	**Development Done on Device Bonder to Address 3D Requirements in a Production Environment** Pascal Metzger, Ph.D., SET Corporation	**Extending Capabilities of Etch and Deposition Technologies for 3D Packaging of MEMS in Volume Production** Chris Jones, SPTS Technologies
5:00 PM	**Recent Advances in Die Attach Film and Temporary Wafer Protection** Frederick Lo, AI Technology	**Thermal Resistant Thin Wafer Support Technology for 3DIC** John Moore, Daetec, LLC	**Fabrication of 3D Microrobotic Parallel Actuator Architecture** Peter Raffensperger, University of Canterbury
	5:30pm - 7:00pm, Exhibit Hall Exhibitor Reception – Hosted by KLA - Tencor		

Sessions at a Glance: Wednesday, November 12th

8:00 AM	**MEMS Plenary: Wearable, Wireless Health Solutions and Related Packaging Challenges** Mehran Mehregany, Ph.D., Case Western Reserve University **OAK BALLROOM (2ND FLOOR)**		
9:00 AM	**9:00 – 9:45am, Exhibit Hall** **Coffee Break**		
	WLP TRACK | MONTEREY ROOM	**3D TRACK | SAN CARLOS ROOM**	**3D TRACK | SANTA CLARA ROOM**
	Session 7 – Wafer-Level Process & Metrology Chair: Jainwen Li, SMIC Co-Chair: Janet Love, Blair-Gordon Associates	**Session 8 – Processing: TSV and Interposers** Chair: Laurette Nacamulli, The Dow Chemical Company Co-Chair: André Rouzaud, CEA LETI	**Session 9 – Metrology** Chair: Maaike M. Visser Taklo, Ph.D., SINTEF Co-Chair: Keith Cooper, SET Corporation
9:45 AM	**Metrology and Inspection for RDL in HVM** Russ Dudley, Rudolph Technologies, Inc.	**Bosch Process Characterization for Donut TSV's** Andy Miller, IMEC	**High Throughput Wafer Edge Inspection and Monitoring for Advanced Wafer Level Packaging** Sumant Sood, KLA-Tencor
10:15 AM	**Enhancing WLCSP Reliability Through Build-Up Structure Improvements and New Solder Alloys** Boyd Rogers, Deca Technologies, Inc.	**300mm Wafer-Scale Through-Silicon Via (TSV) Process With Optimized Backside Reveal and Planarization Methods** Seth Kruger, SUNY Polytechnic Institute	**High Resolution 3D X-Ray Microscopy for the Development of Wafer Level Packaging and 3D IC Integration** Allen Gu, Ph.D., Carl Zeiss X-ray Microscopy, Inc.
10:45 AM	**Automated Wafer-Level Testing of Critical MEMS Parameters using Optical Vibration Measurement** Eric Lawrence, Polytec Inc.	**Analytical and Experimental Studies Of 2.5D Silicon Interposer Warpage: Impact of Assembly Sequences, Materials Selection and Process Parameters** Ron Zhang, Invensas Corporation	**Optical Metrology for High Volume Manufacturing of 3DIC with TSV** Christopher Rosenthal, Lasertec USA Inc.
11:15 AM	**Process Control at Post-Saw for Low-K Wafers** Reza Asgari, Rudolph Technologies, Inc.	**Demonstration of SiC Interposer with High Density and Fine Pitch Microbumps** Melanie Yajima, HRL Laboratories, LLC	**Wafer Overlay Measurement Using Bright-Field Optical Microscopy** Chia-Hung Cho, Industrial Technology Research Institute (ITRI)
11:45 AM	**Lunch Break – Sponsored By Sonix** **Bayshore Foyer**		
1:15 PM	**WLP Plenary - Wafer-Level Packaging Innovations to Enable Wearable Electronics** Theodore (Ted) G. Tessier, FlipChip International, LLC **OAK BALLROOM (2ND FLOOR)OAK BALLROOM**		
	2:15pm– 3:00pm, Exhibit Hall **Refreshment Break – Sponsored by Johnstech International**		
	Exhibition Closes 3:30pm		
	WLP TRACK | MONTEREY ROOM	**3D TRACK | SAN CARLOS ROOM**	**3D-I TRACK | SANTA CLARA ROOM**
	Session 10 - Fan-Out Wafer and Panel-Level Packaging Technologies Chair: Curtis Zwenger, Amkor Technology Co-Chair: Rey Alvarado, Qualcomm	**Session 11 – Electroplating and Metrology** Chair: Steven Xu, Qualcomm Co-Chair: André Rouzaud, CEA LETI	**Session 12 – Integration** Chair: Laurette Nacamulli, The Dow Chemical Company Co-Chair: Keith Cooper, SET Corporation
3:00 PM	**FlexLine™ - A Universal Wafer-Level Packaging Platform for Fan-In and Fan-Out Designs** Rajendra Pendse, Ph.D., STATS ChipPAC, Inc.	**Uniform, Flat, and Interfacial Void Free Deposits for Copper Pillar Applications** Matthew Thorseth, The Dow Chemical Company	**Interposer Based Wide IO-Processor Integration** Andy Heinig, Fraunhofer Institute for Integrated Circuits
3:30 PM	**Panel Based Fan-Out Packaging to Reduce Cost** Klaus Ruhmer, Rudolph Technologies, Inc.	**The Advanced Monitoring of Organic Additives in Copper Electroplating Baths** Micheal Pavlov, ECI Technology	**Cost Comparison of Embedded Die and Wafer Level Packaging** Chet Palesko, SavanSys Solutions LLC
4:00 PM	**Size Does Matter - Breaking the Barriers of Wafer Level Packaging** Adi Merschon, Universal Instruments Corporation	**Non-destructive Acoustic Metrology for Void Detection in TSV's** Robin Mair, Rudolph Technologies, Inc.	**Integrated Tools and Systems to Improve 3DI Manufacturability** Sony Varghese, Micron Technology Inc.
4:30 PM	**Adhesive Enhancement Technology for Directly Metal Plating on Molding Compound** Kenichiroh Mukai, Atotech USA Inc.	**Endoscopes Gain from 3D Assembly and Meticulous Process Control** Phil Marcoux, Promex Industries	**Unique Polymer Coating Process for Improving Performance and Reliability of 3D Wafer Level Packaging** Antun Peic, Ph.D., EV Group
	5:00pm **IWLPC Concludes**		

IWLPC Tutorials | November 13, 2014

T1: Wafer Level Packaging for MEMS and Microsystems Challenges and Opportunities

Leland "Chip" Spangler, Ph.D., Aspen Microsystems, LLC
8:30am-12:00pm | Monterey

OVERVIEW

The ability to package ICs at the wafer-level has been a major contributor to size and cost reduction over the last 10 years. Significant technical challenges had to be overcome to realize these advantages in a production environment. The wafer-level packaging of MEMS and Microsystems also has contributed to the size and cost reduction of those devices, but with greater technical challenges and with a greater reward for overcoming those challenges. This course will review the general requirements for packaging of a variety of MEMS and Microsystem devices and will present methods to meeting those requirements with wafer-level packaging technologies. While research efforts and scientific principles will be at the heart of the discussion, the focus will be on practical implementation of the wafer-level package technology. Case studies will be used to illustrate major concepts. Wafer-level packaged devices covered in the course will include physical sensors such as pressure and inertial sensors, optical sensors and cameras, switches and RF devices as well as fluidic and biomedical devices.

T2: Wafer Level-Chip Scale Packaging (WL-CSP)

Luu Nguyen, Ph.D., Texas Instruments, Inc.
8:30am-12:00pm | Carmel

OVERVIEW

Wafer Level-Chip Scale Packaging (WL-CSP) has gained much success as a packaging form factor in the consumer arena in the past few years that it is almost considered as a "technology commodity." It has been driven by needs for cost reduction, size shrinkage, and enhanced performance. This course will provide an overview of the WL-CSP technology. The market drivers, benefits, and challenges facing industry-wide adoption will be discussed. The standard configurations will be reviewed in terms of their construction, manufacturing process, and published electrical and thermal performance, together with package and board level reliability.

T3: TSV and Other Key Enabling Technologies for 3D IC/Si Integration

John H. Lau, Ph.D., ASM Pacific Technology
1:30pm-5:00pm | Monterey

OVERVIEW

3D IC packaging and 3D IC integration are different. In general, the TSV (through-silicon via) separates 3D IC packaging from 3D IC integration because the latter use TSVs, but 3D IC packaging does not. TSV is the heart of 3D IC integration. It provides the opportunity for the shortest chip-to-chip, and the smallest pad size and pitch of interconnects. The potential high volume manufacturing of 3D IC integration is: (1) memory-chip stacking, (2) wide I/O memory (or logic-on-logic), (3) wide I/O DRAM, wide I/O 2, HMC, and HBM, and (4) wide I/O interface (or 2.5D IC integration). In this presentation, the supply chains and the critical steps such as FEOL, MOL, BEOL, TSV, MEOL (middle-end-of-line), assembly, and test and their ownerships for high-volume manufacturing for those four groups of 3D IC integration will be discussed. The 3D IC packaging, which has been keeping 3D IC integration away from volume production, will be briefly mentioned first. Key enabling technologies such as TSV forming and filling, front and backside metallization, RDL, temporary bonding and de-bonding, and microbumping, assembly and reliability will be presented and discussed. All the materials are based on the papers and books published by the lecturer and others in the past three years.

T4: Achieving High Reliability for Lead-Free Solder Joints - Materials Consideration

Ning-Cheng Lee, Ph.D., Indium Corporation
1:30pm-5:00pm | Carmel

OVERVIEW

This course covers the detailed material considerations required for achieving high reliability for lead-free solder joints. The reliability discussed includes joint mechanical properties, development of type and extent of intermetallic compounds (IMC) under a variety of material combinations and aging conditions and how those IMCs affect the reliability. The failure modes, thermal cycling reliability, and fragility of solder joints as a function of material combination, thermal history, and stress history will be addressed in details, and novel alloys with reduced fragility will be presented. Electromigration and tin whisker will also be discussed. The emphasis of this course is placed on the understanding of how the various factors contributing to the failure modes, and how to select proper solder alloys and surface finishes for achieving high reliability. Also will be presented are the desirable future alloys and fluxes in order to meet the challenge of miniaturization.

Registration is still open for Tutorials.
Please visit the registration desk to pre-register ($350/course) before 12:00pm on Wednesday, November 12th.

THANK YOU TO OUR 2014 TECHNICAL COMMITTEE

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Technical Chair: Steven Xu, Ph.D., *Qualcomm*

3D Integration

Peter Ramm, Ph.D., *Fraunhofer EMFT*, 3D Chair
Laurette Nacamulli, *The Dow Chemical Company*, 3D Co-Chair
Thibault Buisson, *Yole Développement*
John Lau, Ph.D., *ASM Pacific Technology*
Zhaozhi(George) Li, Ph.D., *Intel ATTD*
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Wafer-Level Packaging

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Curtis Zwenger, *Amkor Technology,* Co-Chair
Jianwen Li, *Amkor*
Janet Love, *Blair-Gordon Associates*
Luu Nguyen, Ph.D,, *Texas Instruments*
Gilles Poupon, *CEA-LETI Minatec*
Yi Qin, Ph.D., *The Dow Chemical Company*
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Ted Tessier, *Flip Chip International*
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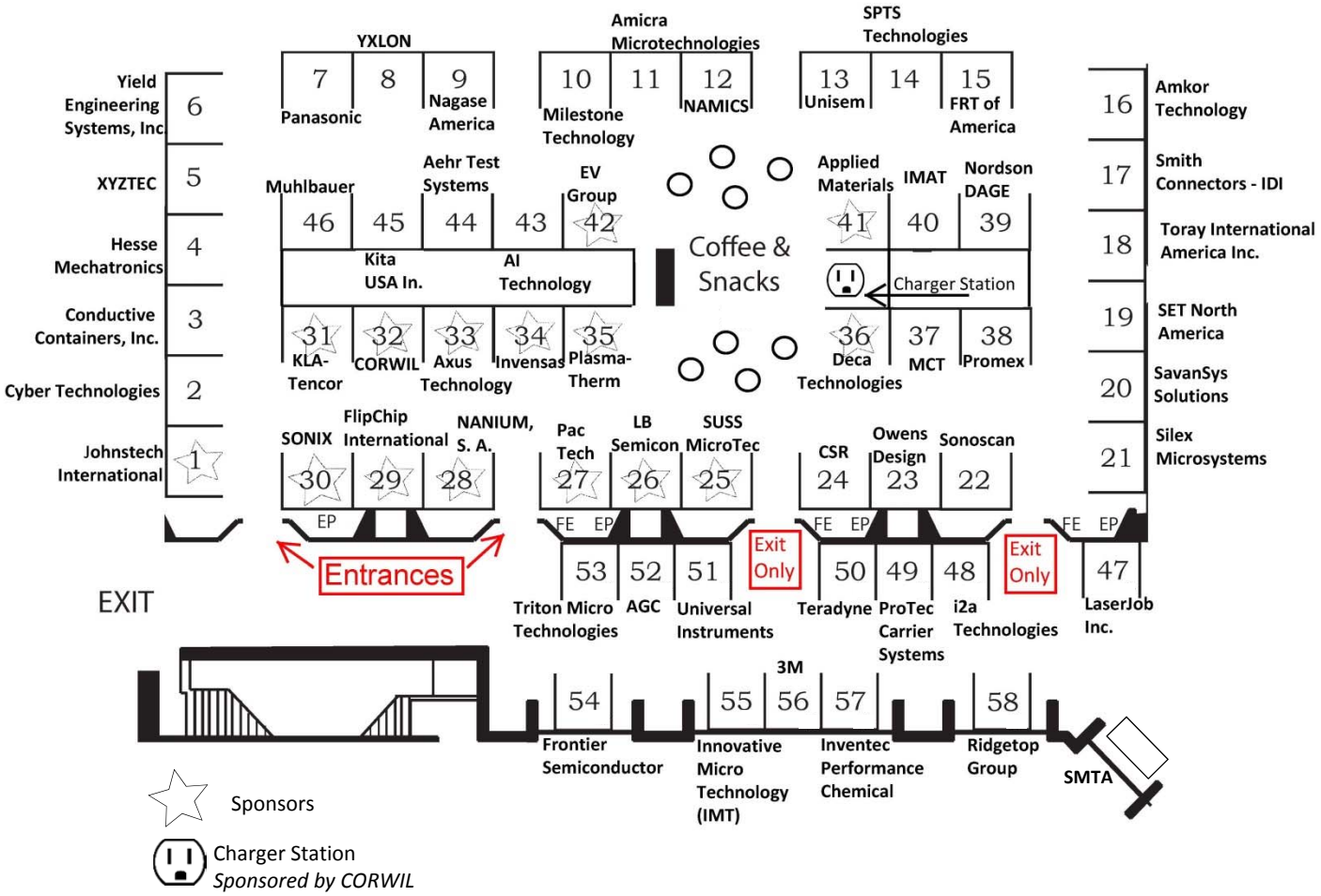
NOVEMBER 11-13, 2014

2014 IWLPC Exhibtion Floor Plan



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Visit the Chip Scale Review Booth (#24) to enter to win a GoPro HERO3+!

Visit the SMTA Silicon Valley Chapter in the Registration Foyer to enter to win VISA gift cards!

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3M Tape & Reel Products provide a variety of carrier and cover tape packaging solutions for WLCSP packages.

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Booth No: 44

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Amkor Technology Inc.

Booth No: 16

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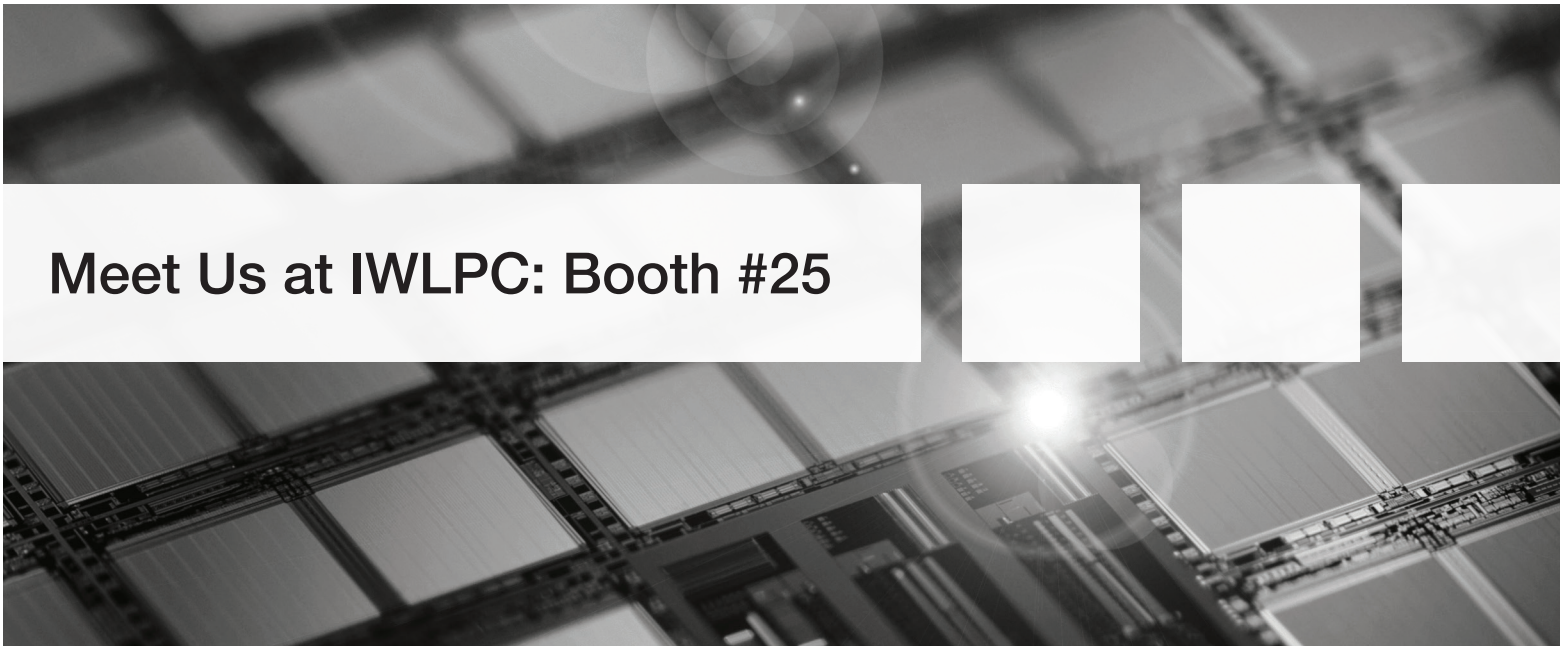

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PLEASE NOTE:

SESSION 2 - 3D Track

11:15 am

Room Temperature Temporary Bonding/ Debonding Processes for 2.5/3D Integration

Tim McCrone, SUSS MicroTec

Co-Authors: Robert Hergert, Gary Choquette

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Chip Scale Review

Booth No: 24

IWLPC Co-organizer

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Founded in 1997, Chip Scale Review covers device and wafer-level test, assembly, and packaging. While holding true to its founding mission, as packaging has evolved, so too has CSR, which now also covers high-density interconnection technologies including 3D packages, MEMS, and other wafer-fabricated devices. We're proud to be part of an industry that has been responsible for most of the major technological breakthroughs since the "birth" of the integrated circuit. Be sure to visit us during the expo at the Chip Scale Review booth.

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Booth No: 29

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Hesse Mechatronics, Inc.

Booth No: 4

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Fax: 484-231-3232
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World leader in wedge wire bonding technology for power, automotive, medical, aerospace, RF, microwave, opto, military and consumer electronics, Hesse Mechatronics designs and manufactures thin wire bonders for aluminum and gold, and heavy wire bonders for aluminum, gold and copper, round wire and ribbon, including HCR™ (High Current Ribbon). They also provide wire bonding equipment training, applications support, development and production of prototypes and pre-production manufacturing in four applications and demonstration labs throughout the USA.

i2a Technologies

Booth No: 48

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i2a Technologies provides variety of interconnect services by applying its technologies which enables improvements in the electrical, thermal and mechanical properties of materials and interconnect.
i2a builds products based on that technology, enabling them to produce semiconductor chips and modules that are smaller and faster, and incorporate more features. These semiconductors are utilized in a broad range of electronics products as well as markets (Medical, Mil-Aero, Aerospace, Communication, Automotive, Commercial etc), including digital audio players, digital cameras, personal computers, personal digital assistants, video game consoles and mobile phones. We achieve these benefits without sacrificing reliability by allowing movement within the package and modules, thus addressing critical problems associated with thermally-induced stress which can occur when packages decrease in size. i2a technologies also enable our customers to package semiconductor chips and micro-devices at the wafer level ("wafer level packaging" or "WLP") and to create high-density interconnections between electronic components using glass interposers and flexible substrate materials . Our key services include WLCSP, micro-bumping, interposer, SIP, Flip-chip in variety of package families such as BGA, QFN, QFP and others.
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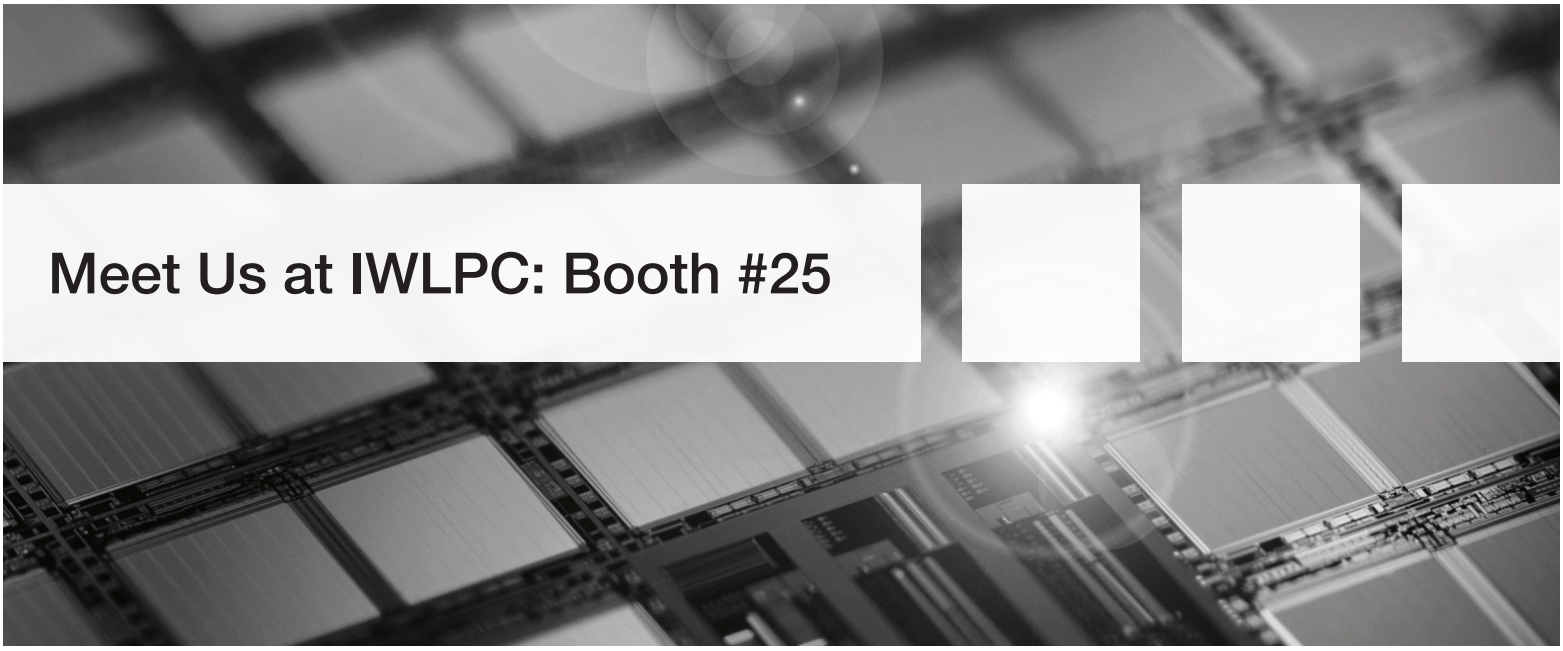

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PLEASE NOTE:

SESSION 2 - 3D Track

11:15 am

Room Temperature Temporary Bonding/ Debonding Processes for 2.5/3D Integration

Tim McCrone, SUSS MicroTec

Co-Authors: Robert Hergert, Gary Choquette

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IMAT, Inc.
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Innovative Micro Technology (IMT)
Booth No: 55

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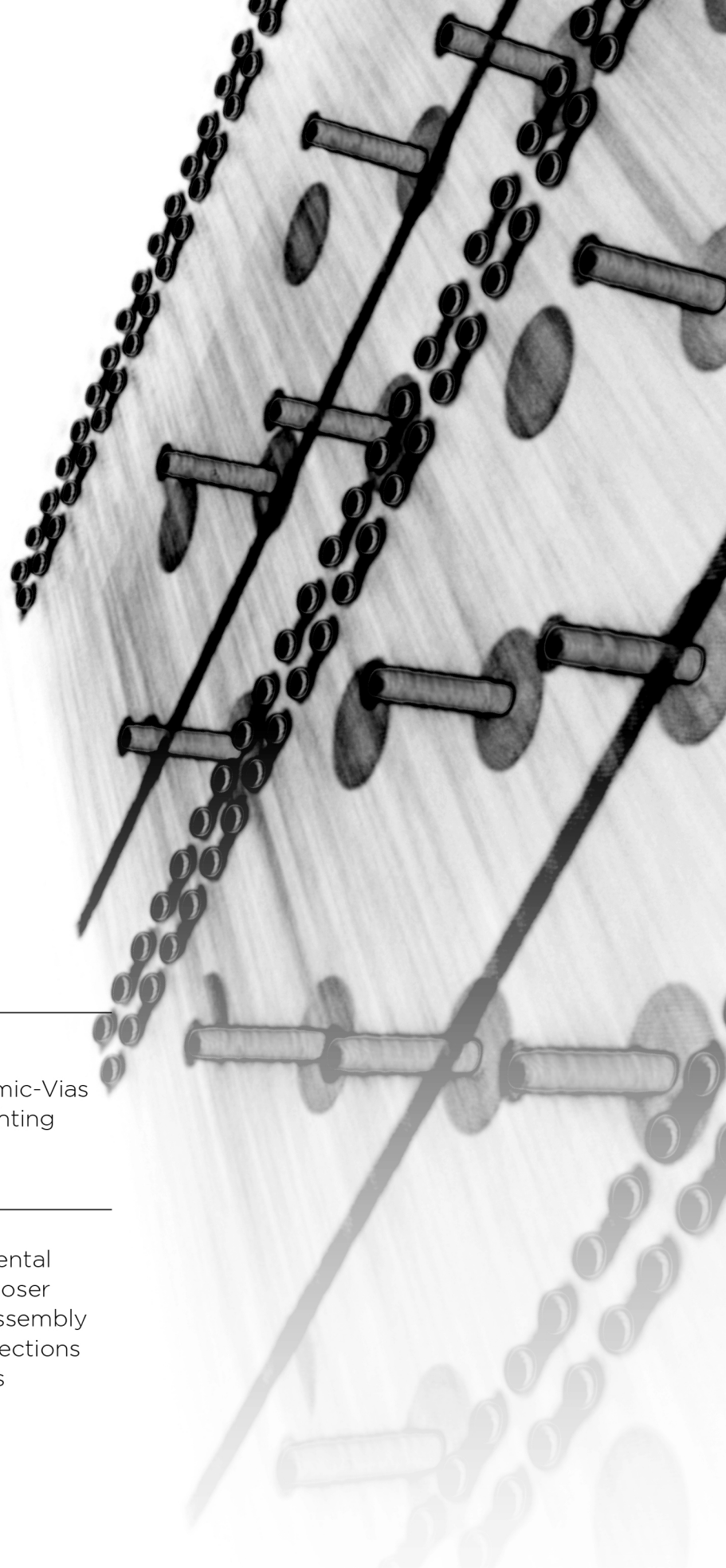

Technology Exhibit Booth #34

Presentations:

3D Track

November 11
10:15 am

Addressing Critical Assembly Challenges in 2.5D and 3D IC Assembly

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WLP Track

November 11
4:30 pm

Reconstituted Big-Chip LEDs on Through-Ceramic-Vias for High-Brightness Lighting

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3D Track

November 12
10:45 am

Analytical and Experimental Studies of Silicon Interposer Warpage: Impacts of Assembly Sequences, Material Selections and Process Parameters

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NAMICS
Booth No: 12

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Promex Industries Inc.

Booth No: 38

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Fax: 408-496-0117
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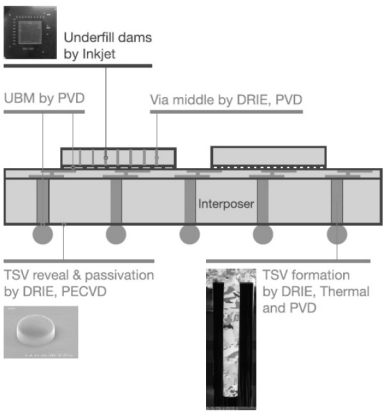
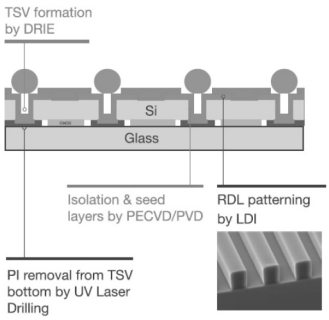
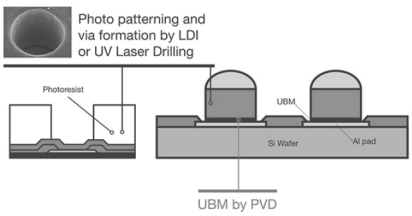


3DWLP



Cu pillar bumps



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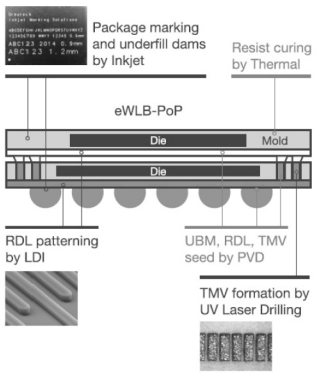

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