



2020

IWLPC

17th Annual

International Wafer-Level Packaging Conference & Exposition

***"Bridging the Boundaries:
Wafer, Panel and Beyond"***

Virtual Conference and Expo

Live Virtual Exposition: October 13-14, 2020

On-Demand Conference & Expo: October 13-30, 2020

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Welcome to the 17th Annual International Wafer-Level Packaging Conference

IWLPC brings together the semiconductor industry's most respected authorities addressing all aspects of Wafer-Level Packaging, 3D Integration and Advanced Manufacturing and Test.

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Executive Team

Tanya Martin, *SMTA*

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Tanja Braun, Ph.D., *Fraunhofer IZM*

Burt Carpenter, *NXP Semiconductors*

Takenori Fujiwara, Ph.D., *Toray Industries, Inc.*

Timo Henttonen, *Microsoft*

E. Jan Vardaman, *TechSearch International, Inc.*

3D Integration Track

John Lannon, Ph.D., *Micross Advanced*

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Thomas Gregorich, *ZEISS Semiconductor Manufacturing Technology*

Zia Karim, Ph.D., *Yield Engineering Systems*

Herb Reiter, *eda 2 asic Consulting, Inc.*

Ted Tessier, *Gordian Semiconductor Packaging Solutions*

Advanced Manufacturing and Test

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Habib Hichri, Ph.D., *Ajinomoto Fine-Techno USA*

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Scott Jewler, *SVXR, Inc.*

Ananthakrishnan Narayanan, Ph.D., *Phononic, Inc.*



Join industry leaders, technologists and innovators for the 17th Annual International Wafer-Level Packaging Conference & Exhibition (IWLPC). The IWLPC is recognized as the premier semiconductor packaging conference and exposition focused on advanced wafer-level packaging technology. This year's conference theme, **"Bridging the Boundaries: Wafer, Panel and Beyond"** reflects the role of advanced wafer-level packaging in the enablement of 5G communications, AI, and IoT, automotive and more.

The IWLPC has always provided a dynamic environment for learning, networking and technical exchange and this year will be no different. Well, maybe a little different. The 2020 conference will be the first IWLPC to be held virtually. The conference committee has arranged for a high-quality virtual conference experience to deliver the technical content and to facilitate communication and networking. As in prior years, the conference comprises of three major parts: the technical program, the professional development courses, and the technology exposition. The technical program has three parallel tracks with over 40 presentations on wafer-level packaging, 3D integration, and advanced manufacturing and test technologies. This year the technical presentations will be available on demand from October 13 through October 30. A chat feature will enable attendees to interact with the speakers, exhibitors and other attendees.

The 2020 IWLPC will kick off with a keynote talk titled "Trends, Challenges, Opportunities in Advanced Packaging for Smart Computing Era" given by Dan Oh, Ph.D., Engineering VP of Test & System Package (TSP), Samsung Electronics. Dr. Oh's speech will be broadcast live on Tuesday, October 13, 2020 at 9:00am US Pacific. In addition, Jan Vardaman of Techsearch will moderate a panel discussion entitled "Meeting Future Advanced Packaging Challenges: What's Next?" This event will be live on Wednesday, October 14 at 9:00am US Pacific. Two professional development courses will also be offered. Finally, the technology exposition this year will feature over 50 leading companies from across the advanced packaging supply chain. Attendees will be able to browse the virtual exhibition hall and engage in live chat sessions with the exhibitors. We look forward to seeing you this October in cyberspace. Let's have another great IWLPC!

**Get to Know the Technical
Committee Members >>**



— Chris Scanlan, *JCET*
IWLPC General Chair



“Bridging the Boundaries: Wafer, Panel and Beyond”



WLP Track

Wafer-Level Package (WLP) is becoming a defacto choice for many applications. The recent advancements in WLP is making this package form a more adaptable and suitable package for automotive application as well, in addition to other applications. The WLP track is covering key technologies: Advanced WLP (SIP, Flex, Glass wafer), Reliability & Metrology, FO-WLP (High density RDL, Panel-level, FoWLP, Processes/ Material (Electroplating, warpage elimination, thermal laser separation).

3D Integration Track

Multi-functional or smart systems based on heterogeneous integration approaches are now driving the next wave of 3D integration innovation. Some application examples include mixed signal analog/RF systems and high-performance sensors or imagers. Successful implementation of these approaches rely heavily on sound designs, reliable die/wafer bonding processes, improved interconnect fabrication processes, and related characterization and test techniques. The 3D integration track has been organized to cover each of these aspects of heterogeneous integration with session papers ranging from die-package-board co-design for 2.5/3D-ICs and WLP to innovations in panel plating and advanced lithography to novel temporary bond and de-bond solutions.

Advanced Manufacturing and Test Track

The Advanced Manufacturing and Test Track remains devoted to bringing together speakers to address key operational challenges in the diverse field of wafer-level packaging (WLP) and panel-level packaging (PLP). The speakers represent academia, equipment suppliers and device manufacturers and have recorded presentations on a variety of topics applicable to R&D phases through high-volume phases of device manufacturing. This track will feature solutions for silicon and glass, new and improved process materials, advances in testing methods, techniques for heterogeneous integration, and concepts for fan-out packaging. Streaming this track will allow tapping into the ideas, experiences and solutions of the speakers, and the virtual Q&A format will allow ample time for all questions to be answered.

Exposition

While full exposition access will be available to attendees October 13-30, the real-time, virtual exposition will take place October 13-14, where the IWLPC will showcase various exhibiting companies; many which are the leaders in the semiconductor packaging and test industry. Attendees will be able to see the latest products and discuss a broad range of services in a virtual interactive environment.

The International Wafer-Level Packaging Conference has become one of the premier forums focused in three key technology areas: Wafer-Level Packaging, 3D Integration and Advanced Manufacturing and Test.

Technical Program

October 13-30

Wafer-Level Packaging (WLP)



600mm Wafer-Level Fan Out on Panel Level Processing with 6-Sided Die Protection
Jacinta Aman Lim, *Nepes*

Advanced Preclean Chamber for UBM/RDL Contact Resistance Improvement in Advanced Node Packaging Application
Clinton Goh, *Applied Materials*

Advanced Si-less Mios Technology for Heterogeneous Integration
Jae-Gwon Jang, *Samsung*

Board Level Reliability of Automotive Grade WLCSP for Radar Applications
Nishant Lakhera, Ph.D., *NXP Semiconductors*

Current Crowding and Stress Effects in WCSP Solder Interconnects: A Simulative and Practical Study About the Effects of Major Electromigration Failure Mechanisms in DC and Pulsed-DC Conditions
Allison Osmanson, *University of Texas at Arlington*

Design Process & Methodology for Achieving High-Volume Production Quality for FOWLP Packaging
Keith Felton & John Ferguson, *Mentor Graphics*

Developments of Low Dielectric Loss Polyimides and Fabrication of Advanced Packagings for 5G Applications
Takenori Fujiwara, Ph.D., *Toray Industries, Inc.*

Electrochemical Plating of Nano-Twinned Cu for WLP Applications
Pingping Ye, Ph.D., *MacDermid Alpha*

Fan-Out Wafer Level Packaging Advanced Manufacturing Solution for Fan-Out WLP/PLP by DFD (Die Face Down) Compression Mold
Yuichi Kajikawa, *TOWA USA Corp.*

High Resolution Dry-Film Photo Imageable Dielectric (PID) Material for FOWLP, FOPLP, and High Density Package Substrates
Chihiro Funakoshi, *TAIYO INK MFG. CO., LTD*

Low-Warpage Encapsulants for Wafer-Level Packaging
Jay Chao, Ph.D., *Henkel Corporation*

Maskless Lithography Optimized for Heterogeneous and Chiplet Integration
Bozena Matuskova, *EV Group*

Physical Verification of Panel-Level Packaging Designs Utilizing Adaptive Patterning Technology
Tarek Ramadan, *Mentor Graphics*

Selective Copper Metallization for Advanced Packaging
Rashid Mavliev, Ph.D., *Ipgrid, Inc.*

Technical Program (Continued)

October 13-30

3D Integration Track



Die to Wafer Hybrid Bonding: Multi-Die Stacking with TSV Integration

Guilian Gao, Ph.D., *Xperi*

EMI Shielding for System in Package using Nozzless Ultrasonic Spray Coating and Silver Particle Free Ink

Stuart Erickson, *Ultrasonic Systems, Inc.*

Hydrogen Embrittlement and Nano Void Classification Within Electroless Copper Depositions

Roger Massey, *Atotech UK*

A Study About Facile Interconnect Formations Involving SB²-Jet Solder Ball Stacking for Colonnade Patterning in Hybrid Package Architectures

Matthias Fettke, *PacTech*

Accelerating Innovations in the New Era of HPC, 5G and High Speed Networking with Advanced 2.5D/3D Packaging

Max Min, Ph.D., *Samsung Foundry*

Active Mold Packaging for Novel Antenna-in-Package Interconnection and Manufacturing

Florian Roick, *LPKF Laser & Electronics AG*

Construction Kit of RF-Blocks in Package Technologies

Andy Heinig, *Fraunhofer IIS - EAS*

Cure Process Impact on Cure Time and Properties of Low Temperature Polyimide for 3D Stacking Applications

Zia Karim, Ph.D., *Yield Engineering Systems*

Machine-Based Learning Methodologies for 3D X-Ray Measurement, Characterization and Optimization of Buried Structures in Advanced IC Packages

Ramanpreet Singh Pahwa, Ph.D., *ASTAR Institute*

Optimization of Low Temperature PECVD Dielectric Stacks for Via-Reveal Passivation

Keith Buchanan, P.E., *SPTS Technologies*

RDL-First FOWLP for Low-Density Applications with RISPAC Technology

Isamu Nishimura, *ROHM Co., Ltd*

Through Glass Vias using an Industry Compatible Glass Handling Solution

David Levy, *Mosaic Microsystems*

Technical Program (Continued)

October 13-30

Advanced Manufacturing and Test (AMT)



Bringing New Life to Glass for Wafer-Level Packaging Applications

Rafael Santos, Ph.D., *LPKF Laser & Electronics AG*

Defect Printability for 2/2 RDL and the Impact of Advanced Reticle Manufacturing Processes

Yang Tong, *Onto Innovation*

Different Layout Fan-Out Panel Level Package (FOPLP) Warpage Profile Handling on Large Area Thermal Chucks

Debbie-Claire Sanchez, P.E., *ERS electronic GmbH*

Efficient & Cost Effective Solutions for Heterogeneous Integration

Glenn Farris, *Universal Instruments Corporation*

Fluxless Soldering in Activated Hydrogen Atmosphere

Gregory Arslanian, *Air Products and Chemicals, Inc.*

Glass in Wafer and Panel-Level Packaging: Changes, Challenges, Hurdles and Barriers

Martin Letz, Ph.D., *SCHOTT AG*

Mask: Key Enabler for Fine Line Patterning in Heterogeneous Integration

Bryan Kasprovicz, *Photonics*

New X-Ray Tubes for Wafer-Level Inspection

Keith Bryant, *Keith Bryant Consultancy*

Non-Surface Contact Approach for Device Flip

Sarah Parrish, *V-TEK, Inc.*

Novel Surface Finish for Next Generation Wafer-Level Packaging Applications

Kunal Shah, Ph.D., *LILOTREE*

Optimizing X-Ray Inspection for Advanced Packaging Applications

Brennan Peterson, Ph.D., *SVXR, Inc.*

Peel Release Temporary Bonding Adhesives for Wafer-Level Processing

Robert Gelosa, *AI Technology, Inc.*

Piezo Dynamic Force Measurement in Advanced Packaging

Robert Hillinger, *Kistler Instrumente AG*

Producing Planarized Uniform Layer in Advanced Photosensitive Polyimide Over Complex Geometry for Fan-Out PLP Applied with a Novel Nozzle-less Spray Coating Technology

Stuart Erickson, *Ultrasonic Systems, Inc.*

Silicon Die Bonding using a Photostructurable Material

Kai Hollstein, *Institute for Microelectronic Systems*

Submicron Lithography Enabling Panel Based Heterogeneous Integration

Doug Shelton, *Canon USA*

Keynote Presentation

Tuesday, October 13 | 9:00am (US Pacific)

Trends, Challenges, Opportunities in Advanced Packaging for Smart Computing Era



Dan Oh, Ph.D.
Engineering VP of the Test & System Package (TSP)
Samsung Electronics
[About the Speaker >>](#)

SAMSUNG

About the Presentation

The AI-driven smart computing era pursues computer performance and reduced power consumption. Advanced packaging technology achieves these goals by integrating logic and memory chips at closer proximities.

This talk portrays how semiconductor technology has evolved from the system integration perspective, and then, it describes some of the future integration schemes which will provide yet another scaling path to modern Silicon-based IC technology. However, extreme integration technology scaling by combining package-level, wafer-level, and fab process-level integration technologies results in problems with high-power density.

To address the challenges in providing power and extracting dissipated heat from highly integrated systems, potential innovative solutions in signal, power, and thermal designs are also examined.

Live Panel Discussion

Wednesday, October 14 | 9:00am (US Pacific)

Meeting Future Advanced Packaging Challenges: What's Next?

As the industry moves into the next silicon nodes and enters the era of heterogeneous integration, packaging plays an increasingly important role. Material selection, design, and fabrication of features, inspection, test, and reliability will be critical. The industry struggles with options to achieve high-density substrate to support high-bandwidth memory (HBM) plus logic. New versions of FO-WLP are being adopted. The panel members will discuss views on the challenges and possible solutions.

Panel Moderator

E. Jan Vardaman, *TechSearch International, Inc.*

Panelists

Tim Olson, *DECA*

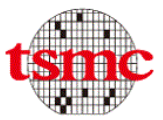
Tanja Braun, Ph.D., *Fraunhofer IZM*

Rahul Manepalli, Ph.D., *Intel Corporation*

Max Min, Ph.D., *Samsung Foundry*

Hong Xie, *Tongfu Microelectronics*

Shin-Puu Jeng, Ph.D., *TSMC*



Professional Development Courses

Tuesday, October 27 | 8:30am-12:00pm (US Pacific)



PDC 1

Polymers in Wafer-Level Packaging

Jeff Gotro, Ph.D., *Innocentrix, LLC*

Overview

The course will provide an overview of polymers and the important structure-property-process-performance relationships for polymers used in wafer-level packaging. The main learning objectives will be: 1) understand the types of polymers used in wafer-level packages, including underfills (pre-applied and wafer applied), mold compounds, and substrate materials 2) gain insights on how polymers are used in Fan Out Wafer-Level Packaging, specifically mold compounds and polymer redistribution layers (RDL) 3) learn the key polymer and processes challenges in Fan Out Wafer-Level Packaging 4) Understand the materials and process challenges for polymer used in panel-level packaging.

Who Should Attend?

Packaging engineers involved in the development, production, and reliability testing of electronic packages would benefit. Those interested in gaining a basic understanding of the role of polymers and polymer-based materials used in electronic packaging will also find this PDC valuable.

Learn
About the
Instructors >>

Thursday, October 29 | 8:30am-12:00pm (US Pacific)



PDC 2

From Wafer to Panel-Level Packaging

Tanja Braun, Ph.D., *Fraunhofer IZM*
Michael Topper, *Fraunhofer IZM*



Overview

Panel-Level Packaging (PLP) is one of the latest trends in microelectronics packing. Besides technology developments towards heterogeneous integration

including multiple die packaging, passive component integration in package and redistribution layer or package-on-package also approach larger substrates formats. These are targeted in this course. Manufacturing is currently done on wafer level up to 12"/300 mm and 330 mm respectively. For higher productivity and therewith lower costs, larger form factors are introduced. Instead of following the wafer level roadmaps to 450 mm, PLP might be the next big step. PLP has the opportunity to adapt processes, materials and equipment from other technology areas. Printed Circuit Board (PCB), Liquid Crystal Display (LCD) or solar equipment is manufactured on panel sizes and offer new approaches also for PLP. However, an easy upscaling of technology when moving from wafer to panel level is not possible. Materials, equipment and processes have to be further developed or at least adapted. This course will give a status of the current Fan-in and Fan-out Wafer-Level Packaging as well as Panel-Level Packaging including Fan-out Panel-Level Packaging substrate embedding approaches. This will include materials discussion, technologies, applications and market trends as well as cost modelling.

Who Should Attend?

Anyone who is interested in Advanced Packaging, Fan-in and Fan-out Wafer-Level Packaging and the transition to Panel-Level Packaging. Engineers and managers are welcome as detailed technology descriptions as well as market trends, applications and cost modelling are presented.



2020 Exposition

Live Virtual Exposition: October 13-14

On-Demand Expo: October 13-30

Reasons Your Company Should Exhibit at IWLPC!

1. Reach a focused international audience
2. Generate exposure in this highly competitive marketplace
3. Share new products and concepts in the market
4. Enhance relationships with existing customers and generate new leads

Exposition:

LIVE Exposition (available 24 hours each day)

Tuesday, October 13 - Wednesday, October 14

On-Demand Exposition

Thursday, October 15 - Friday, October 30

What's Included:

- Private chat with attendees (IM or Video) during Live days
- Direct web link from conference presentations to company booth
- Display company/product videos
- Full analytics and reporting
- Show Directory Listing
- Direct links to social media, news, press, releases and data sheets
- One (1) complimentary conference registration pass (a \$179 value)
- Individual booth raffle/giveaways
- Contact Us page that automatically opens and e-mail message
- Company description
- Opportunity to highlight new products/materials!

Cost:

One (1) Virtual Booth: \$1,000 USD

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As of September 22

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Technical Conference Package

Conference Registration - \$229

Speaker Registration - \$95

Student Registration - \$50 (*Must have a valid '.edu' email*)

Professional Development Courses (\$100 each)

Two Professional Development Courses conducted live, in real-time by several of the most respected individuals in their fields will be offered during the conference.

Note: All prices are listed in USD.

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