Wafer-Level Packaging Symposium

February 15 - 17, 2022
DoubleTree by Hilton San Jose
San Jose, CA, USA

Tuesday, February 15

7:30 AM	**REGISTRATION OPENS**	
9:00 AM	**TUESDAY KEYNOTE** Semiconductor Market Outlook: Market Demand Becomes The Lever that Eases Supply Constraints in 2022 Mario Morales, IDC	
10:00 AM	**BREAK IN THE EXHIBIT HALL**	
	Wafer-Level Packaging Track	**3D Integration Track**
	Session 1	**Session 2**
10:30 AM	**Wafer Level Package Developments for High Performance, Enhanced Reliability Microcontroller Applications** Gaurav Sharma, NXP Semiconductors	**Micro-VeCS Opening Opportunities in WLP and SiP** Joan Tourné, Nextgin Technology
11:00 AM	**Electrochemical Express Analysis of Organic Additives in Lead-Free Wafer Level Packaging Plating Baths** Michael Pavlov, ECI Technology	**MicroLED-Based Opto-Electronic Co-Packaging for Chip-to-Chip Communications** Max Min, Avicena
11:30 AM	**Novel Technology of Enhancing Resolution Limit at the Lithography and Plating Process** Hiiroshi Matsui, Non	**8192-Element Optical Phased Array with Flip-Chip CMOS on Silicon Photonics** Christopher Poulton, Analog Photonics
12:00 PM	**LUNCH**	
	Wafer-Level Packaging Track	**3D Integration Track**
	Session 3	**Session 4**
1:00 PM	**Effective Plasma Treatments for Advanced Wafer Level Packaging** Al Bousetta, Nordson Corporation	**Die-to-Wafer and Wafer-to-Wafer Hybrid Bonding in Spotlight of Heterogeneous Integration** Thomas Uhrmann, EV Group
1:30 PM	**Vacuum Cure Properties of Low Temperature Polyimide LT-S 8300A for FOWLP and FOPLP Applications** Kay Song, Yield Engineering Systems	**Atmospheric Plasma System for In-Line Surface Activation of Die-to-Wafer Direct and Hybrid Bonding** Daniel Pascual, ONTOS Equipment Systems
2:00 PM	**An Organic Cavity Structure for RF-filter by Using High Elastic Modulus Photo-definable Dry film Polyimide** Akira Shimada, Toray Industries, Inc.	**Exposed Die Wafer-Level Molding** Chris Scanlan, BESI
2:30 PM	**BREAK IN THE EXHIBIT HALL**	
3:00 PM	**Next Generation Packaging and Thermal Management With Nanocopper** Randy Stoltenberg, Kuprion Inc.	
3:30 PM	**On-Shoring the Next Generation of Advanced Packaging** Charles Woychik, Skywater Technology	
4:00 PM	**PVD Applications to Enable Heterogenous Integration** Kenton Read, Evatec NA	
4:30PM-6:00PM	**OUTDOOR NETWORKING RECEPTION**	

Wednesday, February 16

7:30 AM	**REGISTRATION OPENS**	
9:00 AM	**WEDNESDAY KEYNOTE** **Advanced Packaging for Silicon Photonics in Hyperscale Data Center Applications** Jie Xue, Cisco	
10:00 AM	**BREAK IN THE EXHIBIT HALL**	
	Wafer-Level Packaging Track	**Adavanced Manufacturing & Test Track**
	Session 5	**Session 6**
10:30 AM	**Study on PVD Degassing Conditions for Fan-out Panel Level Packaging** Cheng-Tar Wu, ESWIN	**Predicting End-of-line Metrology Using Partial Least Squares (PLS)** Pratik Kotcher, Applied Materials Inc.
11:00 AM	**Novel insulation Materials for Fan-Out Packages** Hanae Okuyama, Ajinomoto	**Automated CD Measurement and Defect Detection in High-Density Sub-Surface Package Interconnects** Johannes Ruoff, ZEISS SMT
11:30 AM	**Fan-Out on Substrate Comes of Age** E. Jan Vardaman, TechSearch International, Inc.	**Utilizing Acoustic Microscopy (AM) Techniques for In-line Process/Quality Control of WLPs** Steve Martell, Nordson Sonoscan
12:00 PM	**Chips First or Chips Last – An Ongoing Debate for Chiplets** Benedict San Jose, Deca Technologies, Inc.	**Scalable High-throughput Printing of Micro and Nanoscale Interconnects and Electronics for Heterogenous Integration and Advanced Packaging Applications** Ahmed Busnaina, Northeastern University
12:30 PM	**LUNCH**	
	Wafer-Level Packaging Track	**Adavanced Manufacturing & Test Track**
	Session 7	**Session 8**
1:30 PM	**Advanced FOCoS (Fanout Chip on Substrate) Technology for Chiplets Heterogeneous Integration** Lihong Cao, ASE	**Using the Virtual Identifier Thread for Reliability and Security** Dave Huntley, PDF Solutions
2:00 PM	**Advanced Packaging: HDFO for Next Generation Devices** Suresh Jayaraman, Amkor Technology	**AI/ML for Smart Manufacturing in Advanced Semiconductor Packaging** Dongkai Shangguan, Adapdix
2:30 PM	**A Flexible Approach to Heterogeneous Integration: Advanced Platforms for Cost-Effective Silicon Scaling** Roberto Antonicelli, JCET	**Smart Automation for Wafer-Level Packaging Workshop** Alan Weber, Cimetrix
3:00 PM	**Novel 2.5d RDL Interposer Packaging: a Key Enabler for New Era of Heterogeneous Integration** Seungwook Yoon, Samsung Electronics	**Advanced Manufacturing SPC (Smart Manufacturing)** Aaron Neuhaus, Westren Digital
3:30 PM	**BREAK IN EXHIBIT HALL**	
4:00 PM	**PANEL DISCUSSION: Has FO on Substrate Come of Age?** Moderators: E. Jan Vardaman, TechSearch International, Inc. *This panel will discuss which applications are most suitable for FO on Substrate and what are the alternatives. The panel will also address the challenges and limitations.*	
5:00 PM	**CLOSING COMMENTS**	

Thursday, February 17

	Professional Development Course Options
	PDC1: Alternative Organic Interposer Structures Joe Dickson, WUS PCB Ltd
	PDC2: From Wafer to Panel Level Packaging Tanja Braun, Ph.D., and Michael Topper, Fraunhofer IZM
	PDC3: Fan-out Packaging and Chiplet Heterogeneous Integration John Lau, Ph.D., Unimicron
	PDC4: Polymers in Wafer Level Packaging Jeff Gotro, Ph.D., Innocentrix, LLC