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Emergency Incident Data Document (EIDD) standard”**

NENA PSAP Master Clock Standard



NENA PSAP Master Clock Standard
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National Emergency Number Association
4350 N Fairfax Dr, Suite 750
Arlington, VA 22203-1695
800-332-3911
or: commleadership@nena.org

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The following industry experts and their companies are recognized for their contributions in development of this document.

Issues 1, Issue 2, and Issue 3	
Members:	Company
Billy Ragsdale, Chair, CPE TC	BellSouth
Dorland, Gene, Working Group Leader	Spectracom
Fred Strong	Ameritech
John Hunt	Ameritech
Joe Brozovich	AT&T / Lucent Technologies
Pappas, Rick	Baker Integrated Audio
Joe Morris	Bell Atlantic
Tom Offutt	Bell Atlantic
Hayes, Dave	Bell Atlantic
Terry McLarty	BellSouth
Pierre Brisson	CML
Tonu Busam	CML
Martin Huet	CML
Kevin Sou	CML
Marc Pytura	CML Technologies
Daniel Biage	CML Technologies Inc.
Pierre Coll	CML Technologies Inc.
Tom Ewing	GTE West
Gordon Gipson	IDC
Wein Van de Groep	Interact
Eileen Boroski	Lucent Technologies
Andrew Kendzior	Motorola - SRX
Joe Sallak	Motorola, Inc
Gary Thomas	Motorola, Inc
Michael Vislocky	Network Orange
Bill Bernhardt	NYNEX
Don Cuozzo	NYNEX
John DeLorenzo	NYNEX
Pat Moran	NYNEX
Randy Dalrymple	Orbacom Systems
Richard Frye	Orbacom Systems



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George Caspary	Pacific Bell
Beverly Slocum	Pacific Bell
Bob Tilden	Pacific Bell
Kantu Patel	Pacific Bell
Robert Russo	Pacific Bell
Bob Tilden	Pacific Bell
Jay Fuller	Plant Equipment
Martin Harnois	Plant Equipment
Phil Rotheram	Positron
Bev Slocum	Positron
Albert Israel	Positron Industries Inc.
George Marousis	Positron Industries Inc.
Nelson Davis	PRC
Rick Fried	Proctor
John Camp	SBC
Jim Pharr	SBC
Cindy Clugy	SCC Communications
Tom Meegan	South Western Bell
John Lucas	Sprint
Bob Beckler	SRX
Terry Ryan	TCI
Debbie Guyton	Telcordia
Toni Dunne	Texas 9-1-1 Commission
Donna Messineo	Xtend
Randy Richmond	Zetron
Ryan Joy	Zetron
Issue 4	
Mike Vislocky, Chair CPE Committee	Network Orange, Inc.
Randy Lundin	ESE
William Clark	Masterclock
Mark Fletcher	Nortel
Bev Slocum	Positron
Will Hickey	Spectracom
Paul Myers	Spectracom
Gary Palmer	Verizon



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TABLE OF CONTENTS

1	EXECUTIVE OVERVIEW.....	6
1.1	PURPOSE AND SCOPE OF DOCUMENT	6
1.2	REASON TO IMPLEMENT	6
1.3	BENEFITS	6
1.4	OPERATIONAL IMPACTS SUMMARY.....	6
1.5	DOCUMENT TERMINOLOGY.....	6
1.6	REASON FOR ISSUE.....	7
1.7	REASON FOR REISSUE	7
1.8	DATE COMPLIANCE.....	7
1.9	ANTICIPATED TIMELINE	7
1.10	COSTS FACTORS	7
1.11	COST RECOVERY CONSIDERATIONS	7
1.12	ACRONYMS/ABBREVIATIONS	7
1.13	INTELLECTUAL PROPERTY RIGHTS POLICY	8
1.13.1	<i>General Policy Statement</i>	<i>8</i>
2	MASTER CLOCK DESCRIPTION AND FEATURE DEFINITIONS	9
2.1	RS-232 ASCII TIME CODE.....	10
2.2	IRIG SPECIFICATIONS	11
2.2.1	<i>IRIG Formats.....</i>	<i>12</i>
2.2.2	<i>Signature Control.....</i>	<i>12</i>
2.2.3	<i>IRIG B Output</i>	<i>13</i>
2.2.4	<i>IRIG B General Description.....</i>	<i>13</i>
2.2.5	<i>IRIG E Output</i>	<i>16</i>
2.2.6	<i>IRIG E General Description.....</i>	<i>16</i>
2.2.7	<i>Control Function Field.....</i>	<i>16</i>
2.3	ETHERNET 10/100 BASE-T NETWORK TIME PROTOCOL.....	20

12/21/2016: Superseded by "ANSI/APCO/NENA 2.105.1-2017, APCO/NENA NG 9-1-1 Emergency Incident Data Document (EIDD) standard"

1 Executive Overview

1.1 Purpose and Scope of Document

This Standard is a guide for designers and manufacturers of PSAP equipment. It identifies engineering and technical requirements to be met before the NENA membership shall consider purchase of such equipment; it may also be of value to purchasers, maintainers and users of such equipment.

This document is not intended to provide complete design specifications for a PSAP Master Clock. It will neither ensure the quality of the performance of the equipment nor should it serve as an exclusive procurement specification.

1.2 Reason to Implement

This standard provides a standard method of connecting an accurate time source to the various elements of a PSAPs CPE that depend on time information for operation. When this standard is used to guide the design, development, and acquisition of CPE, successful system integration of the time source equipment with the CPE elements that depend on accurate time is enabled.

1.3 Benefits

Adoption of this Standard enables interoperability among the devices using the interfaces described.

1.4 Operational Impacts Summary

Implementation and management of a standard time source in a PSAP is significantly improved when products are selected that conform to this standard.

1.5 Document Terminology

The terms "shall ", "must" and "required" are used throughout this document to indicate required parameters and to differentiate from those parameters that are recommendations. Recommendations are identified by the words "desirable" or "preferably".

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1.6 Reason for Issue

This document is issued to serve as an industry standard and guide for E9-1-1 PSAP equipment.

1.7 Reason for Reissue

NENA reserves the right to modify this document. Whenever it is reissued, the reason(s) will be provided in this paragraph.

- Issue 2, April 28, 1998, issued to add Glossary of Terms, Acknowledgments, Paragraph 4-Section 2 and update Section 4, Output Signal, Paragraph A and B.
- Issue 3, May 17, 2000, issued to change Paragraph 3 - Section 2 to include an Ethernet interface and add (section 5) describes Ethernet Interface.
- Issue 4, September 22, 2005, issued to add new ASCII data code Format “8” to include 4-digit year information to enhance the original NENA-approved Format “0” that does not include this. This issue also incorporates the current NENA standard template which, among other things, updates NENA’s address.

1.8 Date Compliance

All systems that are associated with the 9-1-1 process shall be designed and engineered to ensure that no detrimental, or other noticeable impact of any kind, will occur as a result of a date/time change up to 30 years subsequent to the manufacture of the system. This shall include embedded application, computer based or any other type application.

To ensure true compliance the manufacturer shall upon request provide verifiable test results to an industry acceptable test plan such as Telcordia GR-2945 or equivalent.

1.9 Anticipated Timeline

The deployment or implementation of this standard will take place as required.

1.10 Costs Factors

The cost factors associated with the adoption of this standard are not determined.

1.11 Cost Recovery Considerations

Normal business practices are assumed to be the cost recovery mechanism.

1.12 Acronyms/Abbreviations

This is not a glossary! See [NENA Master Glossary](#) of 9-1-1 Terminology located on the NENA web site for a complete listing of terms used in NENA documents.

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The following Acronyms are used in this document:	
ASCII	American Standard Code for Information Interchange
BCD	Binary Coded Decimal
GPS	Global Positioning System
IRIG	Inter-Range-Instrumentation Group
NIST	National Institute of Standards and Technology
NTP	Network Time Protocol
SBS	Straight Binary Seconds
SNTP	Simple Network Time Protocol
TTL	Transistor to Transistor Logic
UPS	Uninterruptible Power Supply
USNO	United States Naval Observatory
UTC	Universal Coordinated Time

1.13 Intellectual Property Rights Policy

1.13.1 General Policy Statement

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National Emergency Number Association
4350 N Fairfax Dr, Suite 750
Arlington, VA 22203-1695
800-332-3911
or: commleadership@nena.org

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2 MASTER CLOCK Description and Feature Definitions

To insure consistency of time stamps added to event records, reports and voice recordings, it will be required that equipment such as CAD, ANI/ALI Controllers, Voice Recorders, Radio Consoles, etc., will have the ability to synchronize internal clocks to a PSAP master clock.

The PSAP master clock shall be traceable to Coordinated Universal Time (UTC) and have a continuous accuracy of .1 seconds relative to UTC when locked to the UTC time source. In the event the PSAP master clock becomes unlocked from the external UTC source and must "free run", it will not exceed an error accumulation of more than 1 second per day.

The PSAP master clock system shall have a front panel Display to indicate time and shall have the optional capability to provide time codes via an RS-232 serial, IRIG (Inter Range Instrumentation Group), and Ethernet 10 / 100 Base T interfaces. These interfaces will provide a time code that will be used by the PSAP equipment to synchronize their internal clocks. The master clock must have the capability to automatically adjust the Master Clock Display, RS-232 and IRIG time codes for Daylight Saving Time. It must have a selectable 12 or 24 hour display of Hours, Minutes and Seconds. It must have a means to indicate its status; locked / unlocked and time synchronized or unsynchronized to the external UTC time source. The master clock shall have alarm dry contact closures that are activated upon loss of power or when the clock has lost time synchronization. Optionally, equipment synchronizing to the ASCII time code data may derive alarm status by monitoring the Time Sync Status character within the data stream.

When developing site requirements for a PSAP it is important to consider that the type and number of time code interfaces required for each site will vary according to CPE equipment type, quantity, and manufacturer. The PSAP Master Clock system therefore must be configured accordingly to meet the quantity and types of time code interfaces required.

It is desirable that the PSAP master clock be connected to an uninterruptible power supply (UPS) or be equipped with internal batteries which are continually charged from main power. If equipped with internal batteries, the batteries must be capable of powering the equipment for a minimum of 15 minutes.

Equipment connected to the master clock must maintain a continuous accuracy of $\pm .25$ seconds relative to the PSAP master clock.

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2.1 RS-232 ASCII Time Code

The RS-232 ASCII time code shall be selectable from one of the formats described below. The RS-232 interface shall conform with the specifications described in NENA 04-001 and the baud rate shall be selectable from these speeds: 1200 bps, 2400 bps, 4800 bps, and 9600 bps. A character consists of 1 start bit, 8 data bits, 1 stop bit, and no parity bit.

The ASCII time code is sent in one of two modes:

- The broadcast mode, in which the code is sent once per second at the beginning of the second.
- The response mode in which the code is sent at the beginning of the second following the receipt of a Carriage Return character from the client device.

The ASCII time code must be available on both a bi-directional serial communications port and a broadcast port.

The bi-directional serial port must send time code when requested by the client. The broadcast port shall automatically send time code once per second at the beginning of the second.

Format "8" is the preferred format because it includes the year.

A character consists of 1 start, 8 data, and 1 stop bit, no parity. The data stream contains a time sync status character, day of year, time zone setting, DST/Standard Time Indicator, and the time zone switch setting. Data structures for the formats are shown below:

Format "0"

CR LF I ^ ^ DDD ^ HH:MM:SS ^ DTZ=XX CR LF

Format "1"

CR LFI ^ WWW ^ DDMMYY ^ HH:MM:SS CR LF

Format "8"

CR LF I ^ ^ YYYY ^ DDD ^ HH:MM:SS ^ D±ZZ CR LF

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where:

- : = Colon separator
- ^ = space separator
- ± = Either "+" or "-"
- CR = Carriage Return
- D = Daylight Savings Time indicator (S,I,D,0)
- DDD = Day of Year (001 - 366)
- HH = Hours (00-23)
- I = Time Sync Status (space, ?, *) See description below.
- LF = Line Feed
- MM = Minutes (00-59)
- MMM = JAN|FEB|MAR|APR|MAY|JUN|JUL|AUG|SEP|OCT|NOV|DEC
- SS = Seconds (00 - 60)
- TZ = Time Zone
- WWW = SUN|MON|TUE|WED|THU|FRI|SAT
- XX = Time Zone Offset (in hours, values 00-23)
- YY = Two digit year indication
- YYYY = Four digit year indication
- ZZ = Time Zone Offset (in hours relative to UTC, values 00-12)

The leading edge of the first character (CR) marks the on-time point of the data stream.

Time sync status character I is described below:

- I = (space) when the master clock is synchronized to UTC source.
- = * when the master clock time is set manually.
- = ? when the master clock has not achieved or has lost synchronization to UTC source.

The Daylight Saving Time indicator provides notice whether Standard Time or DST is in effect and warns of upcoming transitional periods. The Daylight Saving Time indicator D is described below:

- D = S during periods of Standard Time.
- = I on the day of the change INTO Daylight Saving Time.
- = D during periods of Daylight Saving Time.
- = O on the day of the change OUT of Daylight Saving Time.

The data is output in a 24-hour time format. The time may be offset to a local time by setting the time zone switches to the appropriate value.

2.2 IRIG Specifications

Signal Type:

- A. IRIG B: B000, B120
- B. IRIG E: E001, E111

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Accuracy: Within 0.3 milliseconds of the on-time pulse.

Output Connector: BNC

Output Signal: Amplitude modulated or pulse width coded, switch selectable.

A. Amplitude Modulated Output:

Signal level shall have a mark to space ratio of 3.3 to 1.

Mark amplitude levels shall be adjustable over a range of 2.0 to 7.0 volts peak to peak into a 600-ohm load.

B. Pulse Width Coded TTL Output:

Open circuit levels: High \geq 4.0 volts

Low \leq 0.6 volts.

Loading: Output TTL-compatible into loads \geq 600 ohms.

The IRIG B or E time code will be in the following format and may be configured as amplitude modulated or pulse width coded.

The IRIG B output contains the Binary Coded Decimal (BCD) and Straight Binary Seconds (SBS) time data per IRIG B specification. The IRIG E output provides BCD data per specification and additionally SBS data in the Control Function Field. A time sync status character and year information shall be encoded in the Control Function Field for both formats.

2.2.1 IRIG Formats

Selectable IRIG formats from the PSAP master clock will be:

IRIG B

IRIG B with Signature Control

IRIG E

IRIG E with Signature Control

The IRIG output will be selectable in either amplitude modulated or pulse width coded.

2.2.2 Signature Control

Signature control removes the time code modulation from the IRIG output whenever the master clock has lost time sync to UTC. Under signature control only the full or mark amplitude carrier will be output for amplitude modulated signals. A TTL logical high will be output for pulse width coded signals. Once the master clock reacquires time sync to the UTC source, the full IRIG output is restored.

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2.2.3 IRIG B Output

The IRIG B output contains BCD and SBS time data per IRIG specifications. The PSAP master clock may output local time by using the time zone offsets.

2.2.4 IRIG B General Description

1. Time frame: 1.0 seconds.
2. Code digit weighting:
 - A. Binary Coded Decimal time-of-year.
Code word - 30 binary digits.
Seconds, minutes hours, and days.
Recycles yearly.
 - B. Straight Binary Seconds time-of-day.
Code word - 17 binary digits.
Seconds only, recycles daily.
3. Code word structure:

BCD: Word seconds digits begin at index count 1. Binary coded elements occur between position identifier elements P₀ and P₅ (7 for seconds, 7 for minutes, 6 for hours, and 10 for days) until the code word is complete. An index marker occurs between decimal digits in each group to provide separation for visual resolution. Least significant digit occurs first.

SBS: Word begins at index count 80. Seventeen Straight Binary Coded elements occur with a position identifier between the 9th and 10th binary coded elements. Least significant digit occurs first.
4. Pulse rates:
 - A. Element rate: 100 per second.
 - B. Position identifier rate: 10 per second.
 - C. Reference marker rate: 1 per second.
5. Element identification: The "on time" reference point for all elements will be the pulse leading edge.
 - A. Index marker (Binary 0 or uncoded element): 2-millisecond duration.
 - B. Code digit (Binary 1): 5-millisecond duration.
 - C. Position identifier: 8-millisecond duration.
 - D. Reference marker, 1 per second. The reference marker appears as two consecutive position identifiers. The second position identifier marks the on-time point for the succeeding code word.
6. Resolution:

Pulse width coded signal: 10 milliseconds.
Amplitude modulated signal: 1 millisecond.
7. Carrier frequency: 1 kHz when modulated.

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Control Function Field

<i>ELEMENT #</i>	<i>C.F. DIGIT #</i>	<i>FUNCTION</i>
50	1	Space
51	2	Space
52	3	Space
53	4	Space
54	5	Space
55	6	Time Sync Status
56	7	Space
57	8	Space
58	9	Space
59	PID P6	Position Identifier
60	10	Years Units Y1
61	11	Years Units Y2
62	12	Years Units Y4
63	13	Years Units Y8
64	14	Space
65	15	Years Tens Y10
66	16	Years Tens Y20
67	17	Years Tens Y40
68	18	Years Tens Y80
69	PID P7	Position Identifier
70	19	Space
71	20	Space
72	21	Space
73	22	Space
74	23	Space
75	24	Space
76	25	Space
77	26	Space
78	27	Space

Figure 2-1 IRIG B CONTROL FUNCTION FIELD

Element 55 is the time sync status bit. Element 55 is a Binary 1 when the master clock is synchronized, and a Binary 0 when unsynchronized.

Year information consists of the last two digits of the current year (94, 95...00 = 2000). Elements 60 through 63 contain the binary equivalent of year units. Elements 65 through 68 contain the binary equivalent of tens of years. All unused control functions are filled with a space (Binary 0).

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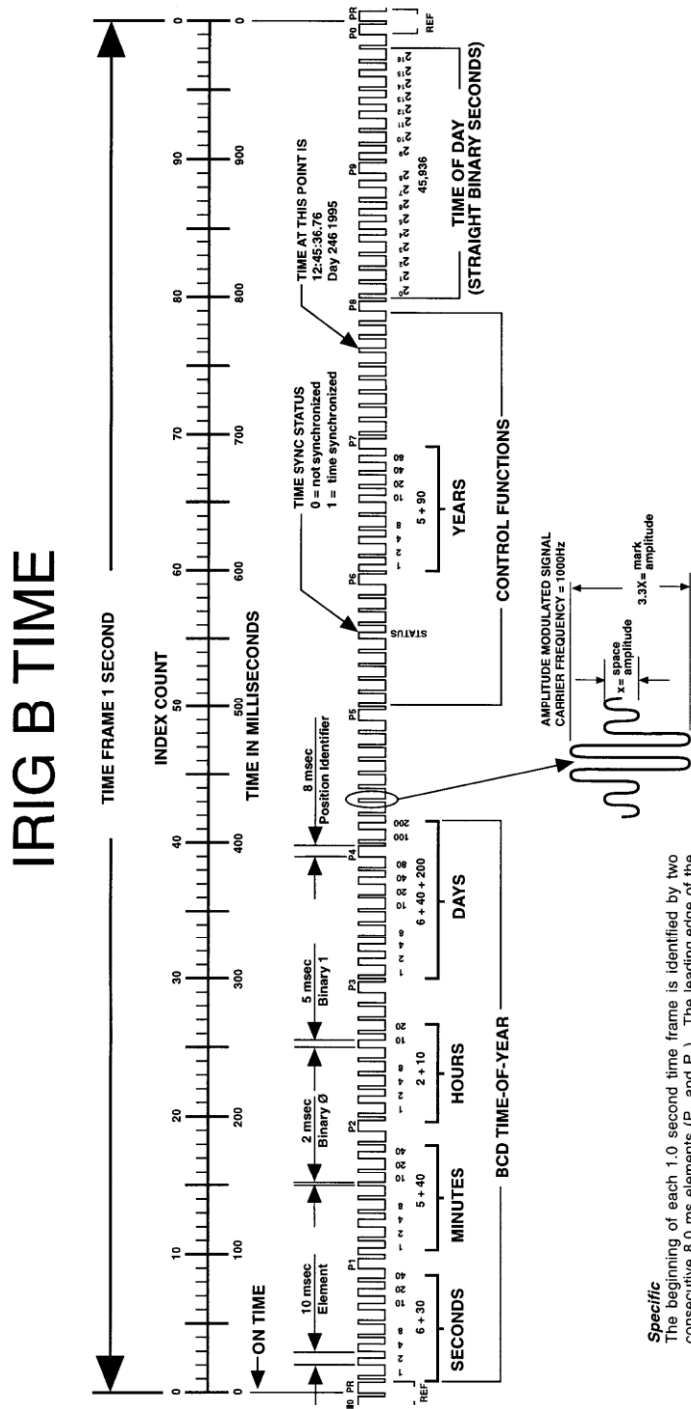


Figure 2-2 IRIG B TIME CODE

Specific

The beginning of each 1.0 second time frame is identified by two consecutive 8.0 ms elements (P_0 and P_1). The leading edge of the second 8.0 ms element (P_1) is the "on time" reference point for the succeeding time code. 10 pps position identifiers P_0, P_1, \dots, P_9 (8.0 ms duration) occur 10 ms before "on time" and refer to the leading edge of the succeeding element.

The two time code words and the control functions presented during the time frame are pulse width coded. The binary "zero" and index markers have a duration of 2.0 ms, and the binary "one" has a duration of 5.0 ms. The leading edge is the 100 pps "on time" reference point for all elements.

The binary coded decimal (BCD) time-of-year code consists of 30 digits beginning at index count 1. The binary coded subword elements occur between position identifiers P_0 and P_9 (7 for seconds; 6 for minutes; 10 for days) until the code word is complete. An index marker occurs between the decimal digits in each subword to provide separation for visual resolution. The least significant digit occurs first. The BCD code recycles yearly.

Twenty-seven control functions occur between position identifiers P_5 and P_9 . Any control function element or combination of control function elements can be programmed to read a binary "one" during any specified number of time frames. Each control element is identified on the Control Function Field Table.

The straight binary (SB) time-of-day code word occurs between position identifiers P_8 and P_9 . Seventeen digits give the time-of-day in seconds with the least significant digit occurring first. A position identifier occurs between the 9th and 10th binary coded elements. The straight binary code recycles every 24 hours.

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2.2.5 IRIG E Output

The IRIG E Output contains BCD time data per IRIG specifications. The PSAP master clock may output local time by using the time zone offsets.

2.2.6 IRIG E General Description

1. Time frame: 10 seconds.
2. Code Digit Weighting:
 - Binary Coded Decimal time of year.
 - Code word - 26 binary digits.
 - Tens of seconds, minutes, hours, and days.
 - Recycles yearly.
3. Code Word Structure: BCD word tens of seconds digits begin at index count 6. Binary coded elements occur between position identifier elements P₀ and P₅ (3 for seconds, 7 for minutes, 6 for hours, and 10 for days) until the code word is complete. An index marker occurs between decimal digits in each group to provide separation for visual resolution. Least significant digit occurs first.
4. Pulse rates:
 - A. Element rate: 10 per second.
 - B. Position identifier rate: 1 per second.
 - C. Reference marker rate: 1 per 10 seconds.
5. Element identification: The "on-time" reference point for all elements is the pulse leading edge.
 - A. Index marker (Binary 0 or uncoded element): 20 milliseconds duration.
 - B. Code digit (Binary 1): 50-millisecond duration.
 - C. Position identifier: 80-millisecond duration.
 - D. Reference marker: 80-millisecond duration, 1 per 10 seconds. The reference marker appears as two consecutive position identifiers. The second position identifier or reference marker is the on time point for the succeeding code word.
6. Resolution:
 - Pulse width coded signal: 0.1 second.
 - Amplitude modulated signal: 0.01 second.
7. Carrier frequency: 100 Hz when modulated.

2.2.7 Control Function Field

IRIG formats reserve a set of elements known as Control Functions (CF) for the encoding of various control, identification, or other special purpose functions. IRIG E has 45 Control Functions located between elements 50 and 98. The master clock uses the control function field to encode year data, time sync status, and SBS time data. Table 4-4 lists the Control Function Field and each element's function.

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Element 55 is the time sync status bit. Element 55 is a Binary 1 when the master clock is synchronized, and a Binary 0 when unsynchronized.

Year information consists of the last two digits of the current year (94, 95...00 = 2000). Elements 60 through 63 contain the binary equivalent of year units. Elements 65 through 68 contain the binary equivalent of tens of years.

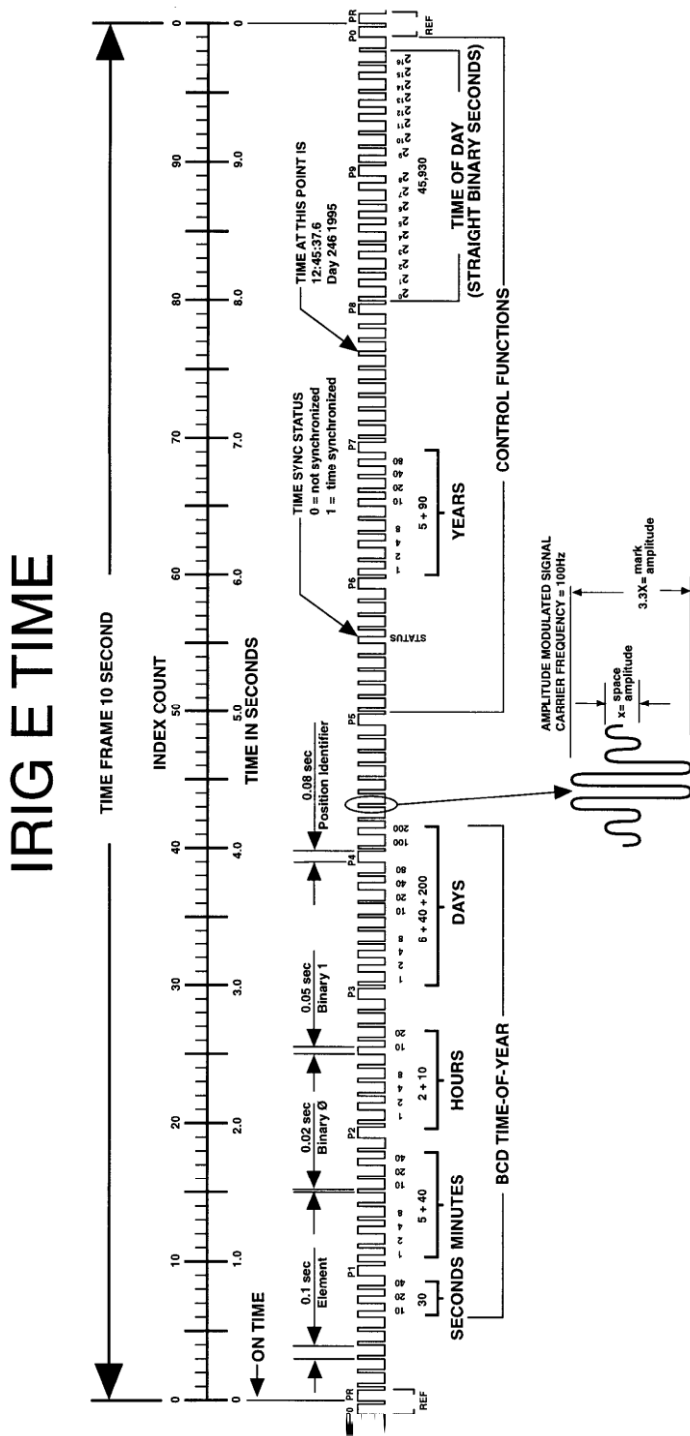
Elements 80 through 97 are encoded with the Straight Binary Seconds (SBS) time data. The SBS time data is incremented in 10-second steps and recycles every 24 hours.

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<i>BIT #</i>	<i>CF ELEMENT #</i>	<i>FUNCTION</i>
50	1	SPACE
51	2	SPACE
52	3	SPACE
53	4	SPACE
54	5	SPACE
55	6	TIME SYNC STATUS
56	7	SPACE
57	8	SPACE
58	9	SPACE
59	PID P6	POSITION IDENTIFIER
60	10	YEAR UNITS Y1
61	11	YEAR UNITS Y2
62	12	YEAR UNITS Y4
63	13	YEAR UNITS Y8
64	14	SPACE
65	15	YEAR TENS Y10
66	16	YEAR TENS Y20
67	17	YEAR TENS Y40
68	18	YEAR TENS Y80
69	PID P7	POSITION IDENTIFIER
70	19	SPACE
71	20	SPACE
72	21	SPACE
73	22	SPACE
74	23	SPACE
75	24	SPACE
76	25	SPACE
77	26	SPACE
78	27	SPACE
79	PID P8	POSITION IDENTIFIER
80	28	SBS 2 ⁰
81	29	SBS 2 ¹
82	30	SBS 2 ²
83	31	SBS 2 ³
84	32	SBS 2 ⁴
85	33	SBS 2 ⁵
86	34	SBS 2 ⁶
87	35	SBS 2 ⁷
88	36	SBS 2 ⁸
89	PID P9	POSITION IDENTIFIER
90	37	SBS 2 ⁹
91	38	SBS 2 ¹⁰
92	39	SBS 2 ¹¹
93	40	SBS 2 ¹²
94	41	SBS 2 ¹³
95	42	SBS 2 ¹⁴
96	43	SBS 2 ¹⁵
97	44	SBS 2 ¹⁶
98	45	SPACE
99	PID P0	POSITION IDENTIFIER

Figure 2-3 IRIG E CONTROL FUNCTION FIELD

12/21/2016: Superseded by "ANSI/APCO/NENA 2.105.1-2017, APCO/NENA NG 9-1-1 Emergency Incident Data Document (EIDD) standard"



The binary coded decimal (BCD) time-of-year code word consists of 26 digits beginning at index count 6. The binary coded subword elements occur between position identifiers P₀ and P₅ (3 for seconds; 7 for minutes; 6 for hours; 10 for days) until the code word is complete. An index marker occurs between the decimal digits in each subword to provide separation for visual resolution. The least significant digit occurs first. The BCD code recycles yearly.

Forty-five control functions occur between position identifiers P₅ and P₀. Any control function element or combination of control function elements can be programmed to read a binary "one" during any specified number of time frames. Each control element is identified on the Control Function Field Table.

Specific
 The beginning of each 10 second time frame is identified by two consecutive 80 ms elements (P₀ and P₁). The leading edge of the second 80 ms element (P₁) is the "on time" reference point for the succeeding time code. 1 pps position identifiers P₀, P₁, ..., P₅ (80 ms duration) occur 0.1 second before 1 pps "on time" and refer to the leading edge of the succeeding element.

The time code word and the control functions presented during the time frame are pulse width coded. The binary "zero" and index markers have a duration of 20 ms, and the binary "one" has a duration of 50 ms. The leading edge is the 10 pps "on time" reference point for all elements.

0

Figure 4-4 IRIG E TIME CODE

12/21/2016: Superseded by “ANSI/APCO/NENA 2.105.1-2017, APCO/NENA NG 9-1-1 Emergency Incident Data Document (EIDD) standard”

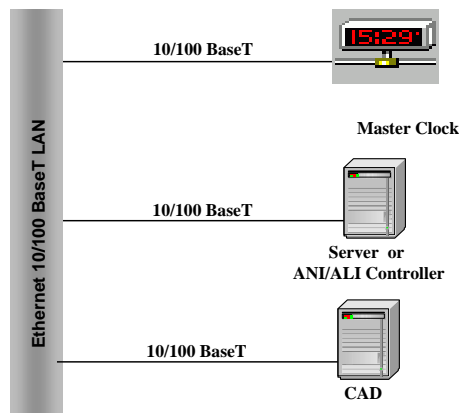
2.3 Ethernet 10/100 Base-T Network Time Protocol

The Ethernet 10/100 Base-T network interface will support NTP (Network Time Protocol) and SNTP (Simple Network Time Protocol). For a complete description of the NTP and SNTP protocols, refer to the Information Sciences Institute RFC: 1305 – NTP and RFC: 2030 – SNTP documents and any subsequent RFC's that supersede these references.

Sample Ethernet Interfaces:

Scenario 1: Integrated Ethernet connection within the Master Clock device

Master Clock - Scenario 1



12/21/2016: Superseded by "ANSI/APCO/NENA 2.105.1-2017, APCO/NENA NG 9-1-1 Emergency Incident Data Document (EIDD) standard"

Scenario 2: External Ethernet connection to the Master Clock device

Master Clock - Scenario 2

